INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPTT./CENTRE: Electronics and Communication Engineering

1. Course Code:	**ECN-561**	Course Title:	**COMPACT MODELING OF SEMICONDUCTOR DEVICES**		
2. Contact Hours:	L: **3**	T: **1**	P: **0**		
3. Exam. Duration(Hrs)	Theory: **3**	Practical: **0**			
4. Relative Weight:	CWS: **20-35**	PRS: **0**	MTE: **20-30**	ETE: **40-50**	PRE: **0**
5. Credits: **4**	6. Semester: **Spring**	7. Subject Area: **PEC**			

5. Pre Requisite: **Fundamentals of semiconductor device physics**

9. Objective: **To introduce students to the field of compact modeling and familiarize them with the tools and methods used in industry-standard compact model development**

10. Details of Course:

S.No.	Contents	Contact Hours
1	Introduction: Introduction to modeling, key differences between different types of models, specific requirements for compact models, use and importance of compact models, familiarization with existing industry-standard compact models and their history	2
2	Modeling fundamentals: Mathematics required for compact modeling, maximum and minimum functions, various types of smoothing functions, continuity and differentiability, convergence criteria, numerical blow-ups, clamping functions, stitching functions, function choice, electrical equivalent circuits, handling differential equations, transient simulations, modeling methodology: semi-empirical, empirical, physical and look-up-table models	5
3	Simulation and Coding: SPICE simulation basics, simulators, coding syntax and practices, Verilog-A details, Verilog-A syntax, Verilog-A coding practices	3
4	Two and three terminal devices: MOSCAP and resistor compact models, relaxation time, terminal current and charges, frequency dependence	4
5	MOSFETs: Compact modeling of MOSFET electrostatics and transport, concept of core model, building a core model, add-on effects, short-channel effects, MOSFET charges, terminal currents and charges, parasitics, frequency dependence, MOSFET model types: surface potential based models, charge based models	6
6	Advanced modeling concepts: binning, binning equations, instance parameters vs model parameters, macro definitions, backward-compatibility and incompatibility, speed/performance, accuracy, noise modeling, self-heating model, non-quasi-static model, quantum effects, band-structure effects, parasitics, ballistic transport, quasi-ballistic transport	8
7	Case study and advanced device effects: Study of industry-standard compact models: BSIMBULK, BSIM-CMG, BSIM-IMG, ASM-HEMT. Introduction to current devices (FinFETs, GAAFETs, FD-SOI, HEMTs) through case study. Discussion on problems encountered in modeling these devices along with solutions adopted at present, scope for improvement	8
8	Magnetic devices: Compact modeling of STT-MRAM, concepts, key criteria for MTJ compact model, tunnel resistance model, switching model, performance criteria, key problems, scope for improvement	3
9	Ferroelectric devices: Compact modeling of ferroelectric materials and devices, NCFETs, L-K equation, domain picture, multi-domain modeling, switching model, MFMIS models vs MFIS models, current scenario, scope for improvement	3
	Total	**42**

11. Suggested Books:

S.No.	Name of Authors/Books/Publishers	Year of Publication/Reprint
1	Y. Tsividis and C. McAndrew,"Operation and Modeling of the MOS Transistor",Oxford Univ. Press	2010
2	C. Hu,"Modern Semiconductor Devices for Integrated Circuits",Pearson	2009
3	Y. S. Chauhan et.al.,"FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG standard",Academic Press	2015
4	C. Hu,"Industry Standard FDSOI Compact Model BSIM-IMG for IC Design",Woodhead publishing	2019
5	G. Gildenblat,"Compact Modeling: Principles, Techniques and Applications",Springer	2010
6	W. Liu and C. Hu,"Bsim4 and Mosfet Modeling For Ic Simulation",World Scientific Publishing Co.	2011
7	W. Liu,"MOSFET Models for SPICE Simulation: Including BSIM3v3 and BSIM4",Wiley-IEEE Press	2001

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–571** Course Title: **SEMICONDUCTOR DEVICE MODELING**

2. Contact Hours: **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): Theory **0 3** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits: **0 3** 6. Semester ✓
Autumn **Spring** **Both**

7. Pre-requisite: **EC –142 and UG – Engineering Mathematics**

8. Subject Area: **PEC and DEC**

9. Objective: The course will provide adequate understanding of semiconductor device modeling aspects, useful for designing devices in electronic, and optoelectronic applications

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Introduction to Numerical Modeling**: Fundamental semiconductor equations, Finite difference scheme, Error analysis, Solution of a system of Linear Equations, Direct Method: LU- decomposition, Tri-diagonal system, Relaxation Method, Numerical solution of Non-Linear Equations: Newton-Raphson method, Finite difference discretization example: Current continuity and energy relations, Introduction to circuit simulations	12
2.	**Modeling of LASER diode**: Rate equations, Numerical schemes: Small signal modeling, and Large signal modeling, Equivalent circuits	7
3.	**MESFET Modeling**: Bridging between time and frequency domains: Harmonic Balance Method, MESFET small signal and large signal equivalent circuit, numerical device simulation and parameter extraction	9
4.	**Quantum Physics Aspects of Device Modeling**: Effective mass Schrödinger equation, Matrix representation, Dirac notation, WKB Approximation, Time dependent and independent perturbation theories, Fermi's golden rule, semi-classical transport in semiconductors: Boltzmann transport equation, numerical scheme, Introduction to Monte Carlo simulations	8

5.	**Introduction to Quantum Effect Device Modeling**: Double barrier resonant tunneling diode, Device modeling through transfer matrix approach, Numerical estimation of diode current density, coupled Poisson-Schrödinger scheme for electron transmission simulations	6
	Total	**42**

11. Suggested Books:

Sl. No.	**Name of Books/ Authors**	**Year of Publicatio**
1.	Selberherr, S., Analysis and Simulation of Semiconductor Devices, Springer-Verlag	1984
2.	Arora, N., MOSFET Models for VLSI Circuit Simulation, Springer-Verlag	1993
3.	C.M. Snowden, and, E. Snowden, Introduction to Semiconductor Device Modeling, World-Scientific	1998
4.	W.J. McCalla, Fundamentals of Computer-Aided Circuit Simulation, Kluwer Academic	1987
5.	Leonard I. Schiff, Quantum Mechanics, Third Edn.,Tata Mc-Graw-Hill	2010
5.	Research papers in specific area	

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–572** Course Title: **MOS DEVICE PHYSICS**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester ✓

Autumn **Spring** **Both**

7. Pre-requisite: **EC - 142**

8. Subject Area: **PEC and DEC**

9. Objective: The course will provide detail understanding of Metal-Oxide-Semiconductor (MOS) Capacitor and allied field effect devices, required for designing VLSI & ULSI CMOS circuits

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**MOS Capacitor**: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges, Midgap gate Electrode, Poly-Silicon contact, Electrostatics of non-uniform substrate doping, ultrathin gate-oxide and inversion layer quantization, quantum capacitance, MOS parameter extraction	10
2.	**Physics of MOSFET**: Drift-Diffusion Approach for IV, Gradual Channel Approximation, Sub-threshold current and slope, Body effect, Pao & Sah Model, Detail 2D effects in MOSFET, High field and doping dependent mobility models, High field effects and MOSFET reliability issues (SILC, TDDB, & NBTI), Leakage mechanisms in thin gate oxide, High-K-Metal Gate MOSFET devices and technology issues, Intrinsic MOSFET capacitances and resistances, Meyer model	15

3.	**SOI MOSFET**:FDSOI and PDSOI, 1D Electrostatics of FDSOI MOS, V_T definitions, Back gate coupling and body effect parameter, IV characteristics of FDSOI-FET, FDSOI-sub-threshold slope,Floating body effect, single transistor latch, ZRAM device, Bulk and SOI FET: discussions referring to the ITRS	7
4.	**Nanoscale Transistors**: Diffusive, Quasi Ballistic & Ballistic Transports, Ballistic planer and nanowire-FET modeling: semi-classical and quantum treatments	6
5.	**Advanced MOSFETs** :Strain Engineered Channel materials, Mobility in strained materials, Electrostatics of double gate, and Fin-FET devices	4
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publicatio
1.	S.M. Sze & Kwok K. Ng, Physics of Semiconductor Devices, Wiley	2007
2.	Yuan Taur & Tak H. Ning, Fundamentals of Modern VLSI Devices, Cambridge	1998
3.	Mark Lundstrom & Jing Guo, Nanoscale Transistors: Device Physics, Modeling & Simulation, Springer	2005
4.	Yannis Tsividis, Operation and Modeling of the MOS Transistor, Oxford University Press	2nd Edn.
5.	J.P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, Springer	1997
6.	Research papers in specific area	

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–573** Course Title: **Digital VLSI Circuit Design**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester ✓

Autumn **Spring** **Both**

7. Pre-requisite: **EC – 142, EC -104, EC - 201**

8. Subject Area: **PCC and DEC**

9. Objective: To acquaint the students with the fundamental concepts of digital VLSI circuit design

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Review of MOSFET operation and CMOS process flow**: MOS Threshold voltage, MOSFET I-V characteristics: Long and short channel, MOSFET capacitances, lumped and distributed RC model for interconnects, transmission lines, CMOS process flow, Layout and design rules.	6
2.	**CMOS inverter**: Static characteristics, power consumption, dynamic	6
3.	**Combinational logic**: Transistor sizing in static CMOS logic gates, static CMOS logic gate sizing considering method of logical effort, dynamic logic, pass-transistor logic, common mode and other cross-coupled logic	6
4.	**Sequential logic**: Static latches and flip-flops (FFs), dynamic latches and FFs, sense-amplifier based FFs, NORA-CMOS, Schmitt trigger, monostable and astable circuits.	8
5.	**Memories and array structures**: MOS-ROM, SRAM cell, memory	6
6.	**Course Project**: SPICE based project on a digital VLSI sub-system design	2
6.	**Timing issues**: Timing fundamentals, clock distribution, jitter, self-timed circuit design, synchronizers and arbiters, basic building blocks of PLLs, clock synthesis and synchronization using PLLs.	8
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publication
1.	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective," Prentics Hall	2003
2.	Sung-Mo Kang, Yusuf Liblebici, "CMOS Digital Integrated Circuits," Tata Mc Graw Hill	2003
3.	R. Jacob Baker, "CMOS Mixed-Signal Circuit Design," Wiley India Pvt. Ltd.	2009
4.	Ivan Sutherland, R. Sproull and D. Harris, "Logical Effort: Designing Fast CMOS Circuits", Morgan Kaufmann	1999

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN-574** Course Title: **Semiconductor Materials, Devices & Characterization**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester ✓
Autumn **Spring** **Both**

7. Pre-requisite: **EC – 142, and UG – Engineering Mathematics**

8. Subject Area: **PCC and DEC**

9. Objective: To provide a thorough knowledge of semiconductor materials, devices and their characterization

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Semiconductor properties**: Crystal structure, intrinsic and doped crystals, excess carriers and current transport.	4
2.	**Band structure of semiconductors**: Band structure, carrier energy and Fermi distributions for free carriers, donor and acceptor impurities, determination of band gap, impurity ionization, and critical temperatures for intrinsic ionization and onset of impurity deionization.	6
3.	**Inhomogeneous impurity distribution**: Impurity diffusion processes and profile derivations, built-in electric field and carrier profiles.	4
4.	**Junction diode**: p-n junction, tunnel diode, quasi Fermi levels, depletion width capacitance and its application in doping profile determination, I-V characteristics of narrow and wide base diodes and their equivalent circuits, breakdown mechanisms, small signal ac impedance.	6
5.	**Bipolar transistor fundamentals**: Formation of transistor, current gains, dc and low frequency characteristics, base resistance and power gain, drift and graded base transistors.	6
6.	**Surface field effect transistors**: Surface states, measurement of surface charge, Q-V/I-V characteristics and equivalent circuit models of MOS capacitor and MOSFET.	6
7.	**Metal-semiconductor junctions**: Rectifying and ohmic contacts, role of surface states, application in energy level characterization; Comparison of p-n junction and Schottky diodes.	6
8	**Pressure effects**: Dependence of energy bandgap on pressure, evaluation of energy pressure coefficients, direct-indirect conversion and identification of defect levels.	4
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publication
1.	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective," Prentics Hall	2003
2.	Sung-Mo Kang, Yusuf Liblebici, "CMOS Digital Integrated Circuits," Tata Mc Graw Hill	2003
3.	R. Jacob Baker, "CMOS Mixed-Signal Circuit Design," Wiley India Pvt. Ltd.	2009
4.	Ivan Sutherland, R. Sproull and D. Harris, "Logical Effort: Designing Fast CMOS Circuits", Morgan Kaufmann	1999

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–575** Course Title: **Microelectronics Lab -1**

2. Contact Hours**:** **L: 0** **T: 0** **P: 3**
3. Examination Duration (Hrs.): **Theory 0** **Practical 03**

4. Relative Weight: CWS 00 PRS 100 MTE 00 ETE 00 PRE 00

5. Credits**:** **2** 6. Semester: **Autumn** 7. Subject Area: **PCC**

8. Pre-requisite: **EC - 142**

9. Objective: To provide knowledge of characterization of devices and fabrication techniques.

10. Details of the Course:

Sl. No.	**Contents**	**Contact Hours**
	Study of Hall effect in semiconductors. (1) Four probe method for resistivity and bandgap measurement of semiconductors. (1) Study of Magneto resistance in semiconductors. (1) I-V characteristics of devices with variation in temperature.(1) C-V characteristics of p-n junction and MOS capacitor.(1) Device characteristics of LED, lasers and solar cells. (3) Study of working of diffusion furnace. (1) Fabrication and characterization of Schottky diodes. (1) Deposition of thin films using physical vapor deposition (vacuum evaporator) and spin coating techniques. (1) MOSFET process/device simulation and parameter extraction. (1)	14x3
	Total	**42**

11. Suggested Books:

Sl. No.	**Name of Authors / Books / Publishers**	**Year of Publication/Reprint**
1.	Lindmayer, J. and Wrigley, C. Y., "Fundamentals of Semiconductor Devices", D.Van Nostrand Co.	2004
2.	Streetman, B.G. and Banerjee, S., "Solid State Electronic Devices", 6th Ed., Prentice Hall of India.	2008
3.	Tyagi, M.S., "Introduction to Semiconductor Materials and Devices", John Wiley & Sons.	1991

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–576** Course Title: **Simulation Laboratory - 1**

2. Contact Hours**:** **L: 0** **T: 0** **P: 3**
3. Examination Duration (Hrs.): **Theory 0** **Practical 03**

4. Relative Weight: CWS 00 PRS 100 MTE 00 ETE 00 PRE 00

5. Credits**:** **2** 6. Semester: **Autumn** 7. Subject Area: **PCC**

8. Pre-requisite: **EC – 142, EC -104, EC - 201**

9. Objective: To provide hands-on experience on the behavioral and structural modeling in a Hardware Description Language (HDL), SPICE circuit simulation and layout.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1	HDL based (1) Behaviour and structural modeling of a VLSI sub-system in a HDL. (2) Implementation and analysis of the sub-system of (1) in IC Compiler.	
2	SPICE and Layout (1) Layout of an optimally sized CMOS combinational circuit driving a large load. (2) Extraction and SPICE simulation of the layout in (1)	14 x 4
	Total	**56**

11. Suggested Books:

Sl. No	Name of Books/ Authors	Year of Publication
1.	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated	2003
2.	R. Jacob Baker, H. W. Li, D. E. Boyce, "CMOS, Circuit Design, Layout,	1997
3.	Bhasker, J., "A VHDL Primer," Pearson India.	2005

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–577** Course Title: **VLSI Technology**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **EC - 142**

8. Subject Area: **PCC and DEC**

9. Objective: To provide knowledge of various processes and techniques for VLSI fabrication technologies.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Introduction to VLSI technology:** Device scaling and Moore's law, basic device fabrication methods, alloy junction and planar process.	4
2.	**Crystal growth:** Czochralski and Bridgman techniques, Characterization methods and wafer specifications, defects in Si and GaAs.	4
3.	**Oxidation: Surface passivation using oxidation.** Deal-Grove model, oxide characterization, types of oxidation and their kinematics, thin oxide growth models, stacking faults, oxidation systems.	4
4.	**Diffusion and ion-implantation:** Solutions of diffusion equation, diffusion systems, ion implantation technology, ion implant distributions, implantation damage and annealing, transient enhanced diffusion and rapid thermal processing.	6
5.	**Epitaxy and thin film deposition:** Thermodynamics of vapor phase growth, MOCVD, MBE, CVD, reaction rate and mass transport limited depositions, APCVD/LPVD, equipments and applications of CVD, PECVD, and PVD.	5
6	**Etching:** Wet etching, selectivity, isotropy and etch bias, common wet etchants, orientation dependent etching effects; Introduction to plasma technology, plasma etch mechanisms, selectivity and profile control plasma etch chemistries for various films, plasma etch systems.	4
7	**Lithography:** Optical lithography contact/proximity and projection printing, resolution and depth of focus, resist processing methods and resolution enhancement, advanced lithography techniques for nanoscale pattering, immersion, EUV, electron, X-ray lithography.	5
	Total	**32**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publicatio
1.	Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall.	2000
2.	Sze, S.M., "VLSI Technology", 4th Ed., Tata McGraw-Hill.	1999
3.	Chang, C.Y. and Sze, S.M., "ULSI Technology", McGraw-Hill.	1996
4.	Gandhi, S. K., "VLSI Fabrication Principles: Silicon and Gallium Arsenide", John Wiley and Sons.	2003
5	Campbell, S.A., "The Science and Engineering of Microelectronic Fabrication", 4th Ed., Oxford University Press.	1996

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN – 578** Course Title: **Digital System Design**

2. Contact Hours**:** **L: 3** **T: 0** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 3** 6. Semester ✓

Autumn **Spring** **Both**

7. Pre-requisite: **Digital Logic Design or Equivalent**

8. Subject Area: **PCC**

9. Objective: To acquaint with the hardware description languages such as VHDL/Verilog for understanding the principles for designing digital and embedded systems.

10. Details of the Course:

Sl.No.	Contents	Contact Hours
1.	**Introduction to Digital and Embedded systems design:** Digital Design Using ROMs, PLAs and PLAs, BCD Adder, 32 - bit adder, A shift and add multiplier, Array multiplier, and Binary divider. Introduction to Embedded system, Design cycle in the development phase for an embedded system, Use_ of target system or its emulator nd In-circuit emulator, Use of software tools for development of an ES.	4
2.	**Hardware Description Languages (HDL):** Digital system Design Process, Hardware Description Languages, Hardware Simulation, Hardware Synthesis, Levels of Abstraction, Characterizing Hardware Languages, Objects and Classes, Signal Assignments, Concurrent and Sequential Assignments.	6
3.	**Design Organization and Parameterization:** Definition and usage of Subprograms, Packaging Parts and Utilities, Design Parameterization, Design Configuration, Design Libraries. Type Declarations and Usage, Operators, Subprogram Parameter Types and Overloading, Other Types and Types Related Issues, Predefined Attributes, User Defined Attributes. Dataflow Description: Multiplexing and Data Selection, State Machine Description, Three State Bussing. Behavioral Description of Hardware: Process Statement, Assertion Statement, Sequential Wait Statements, Formatted ASCII I/O Operations, IC Design Flow. Practical Designs	8

4.	**EPGA Architecture:** Designing and Implementation of Finite State Machines for FPGA; Synthesis Techniques nd Timinig Analysis; Placement and Routing; Embedded Hardware and Software Design with FPGA.	**8**
5.	**DSP Processor Architecture:** Architecture; Functional Units; Fetch and Execute Packets; Pipelining; Registers; Linear and circular Addressing Modes; Instruction Set Assembler Directives for TMS320C6x or ADSP21xx; Linear Assembly; ASM statement within C; C-Callable Assembly Function; Timers; interrupts; Multichannel Buffered Serial Ports; Direct Memory Access; Memory Considerations; Fixed and Floating Point Format Code Improvement ; Constraints Programming Examples Using : C, Assembly, and Linear Assembly.	**8**
6.	**ARM Architecture and Organization:** ARM Assembly Programming; THUMB Assembly Programming; ARM-THUMB Interworking; Assembly and C Mixed Programming; Exception Handling; ARM Tool chain (Assemblers, Compilers, Linkers & Debuggers); Firmware Programming; Cache & MMU; Peripheral Programming; ARM Cortex family of Processors and architecture; Operating modes, Registers and Memory Map of Cortex-M3; Embedded OS; Porting of Embedded OS on ARM.	**8**

11. Suggested Books:

Sl.No.	**Name of Books/Authors**	**Year of Publication**
1.	Embedded System Design: Embedded System Foundations of Cyber- Physical Systems by Peter Marwedel, Springer	2010
2.	Embedded System Design: A Unified Hardware/Software introduction by Frank Vahid, Tony Givargis, John Wiley & Sons, Inc.	2001
3.	Fundamental of Logic Design - Charles H. Roth, and Larry L. Kinney, Brooks/Cole Inc.	2014
4.	Digital Logic and Microprocessor Design with VHDL, Enoch O. Hwang, Publisher- Thomson/Nelson	2006
5.	Digital Design and Computer Architecture, David Money Harris and Sarah L. Harris, Elsevier.	2012
6.	VHDL for Programming Logic, Kevin Skahill, Person Education	2004
7.	ARM System-on-Chip Architecture, Furber, S., 2nd ed. Pearson Education.	2000
8.	DSP Applications Using C and the TMS320C6x DSK, Rulph Chassaing, John Wiley & Sons, Inc.	2002

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code**: EC – 579** Course Title**: Foundations of Semiconductor device physics**

2. Contact Hours: **L: 3 T: 1 P: 0**

3. Examination Duration (Hrs.): **Theory** 0 | 3 **Practical** 0 0

4. Relative Weight**:** **CWS** 15 **PRS** 00 **MTE** 35 **ETE** 50 **PRE** 00

5. Credits**:** 0 | 4 6. Semester √ **Autumn** ☐ **Spring** ☐ **Both**

7. Pre-requisite**: None**

8. Subject Area**: PCC and DEC**

9. Objective: To instigate fundamental concepts of solid state physics and basic semiconductor devices.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Basic Semiconductor properties**: Brief history of semiconductor revolution; types of semiconductor; crystal structure analysis – unit cell, Bravais Lattice, Miller Indices.	3
2.	**Review of quantum mechanics and energy-band theory**: Quantum concepts; basic formalism – particle in a 1-D box, finite potential well; Bloch Theorem; One dimensional analyses of semiconductors – K-P model, Brillouin zone; extrapolation of these concepts to three dimensions.	8
3.	**Equilibrium carrier statistics and R-G processes**: Density of states in 1D, 2D and 3D systems; Fermi-Dirac distribution, FD integral; Maxwell-Boltzmann approximation; equilibrium carrier concentration. Mass-action law; calculation of fermi level in intrinsic, extrinsic and freeze-out conditions; Degenerate semiconductors; recombination-generation (R-G) statistics; surface R-G processes;	7
4.	**Carrier transport:** carrier drift – mobility, narrow dimension effects, scattering phenomenon velocity saturation; diffusion current; Einstein relationship; Quasi-fermi levels, continuity equation; tunneling mechanisms. resistivity, Hall effect	7
5.	**Theory of P-N junction and metal-semiconductor junctions**: electrostatics – built in potential, depletion approximation, Poisson's equation; forward and reverse bias; ideal diode I-V characteristics; breakdown mechanisms; high injection effects; transient and A-C conditions;	7

	Metal-semiconductor junctions - Schottky, ohmic and rectifying contacts; semiconductor heterojunctions, Quantum well structures.	
6.	**MOS capacitor**: Ideal Si/SiO2 MOS capacitor – solution of Poisson's equation, depletion approximation, HFCV, LFCV, deep depletion; non-ideal MOS capacitor - work-function difference, oxide and interface charges, polysilicon depletion effect, quantum effects, tunneling through the insulator.	10
	Total	**42**

11. Suggested Books:

Sl. No.	**Name of Books/ Authors**	**Year of Publication**
1.	Robert F. Pierret, "Advanced Semiconductor Fundamentals," Pearson Prentice Hall.	2002
2.	Robert F. Pierret, "Semiconductor Device Fundamentals," Pearson.	2006
3.	Ben G. Streetman and Sanjay K. Banerjee, "Solid State Electronic Devices," Pearson Education India Pvt. Ltd.	2015
4.	Donald A. Neamen, "Semiconductor Physics and Devices", McGraw Hill Higher Education	2002
5	S. M. Sze and Kwok K. Ng, "Physics of Semiconductor Devices," Wiley	2008
6	Mark Lundstrom, "Fundamentals of Carrier Transport," Cambridge University Press	2009
7	K. Seeger, "Semiconductor Physics," Springer	2004

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–581** Course Title: **Analog VLSI Circuit Design**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester ✓
Autumn **Spring** **Both**

7. Pre-requisite: **EC142 and EC-201**

8. Subject Area: **PEC and DEC**

9. Objective: To acquaint the students with basic CMOS analog building blocks and sub-system design.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Introduction**: Motivation for analog VLSI and mixed signal circuits in CMOS	1
2.	**CMOS device fundamentals**: Basic MOS models, device capacitances, parasitic resistances, substrate models, transconductance, output resistance, f_T, frequency dependence of device parameters.	3
3.	**Single stage amplifiers**: Common source amplifier, source degeneration,	5
4.	**Differential Amplifiers**: Basic differential pair, common mode response, differential pair with MOS loads, Gilbert Cell, device mismatch effects, input offset voltage.	4
5.	**Current Mirrors, Current and Voltage Reference**: Basic current mirrors, cascode current mirrors, active current mirrors, low current biasing, supply insensitive biasing, temperature insensitive biasing, impact of device mismatch.	4
6.	**Frequency Response of Amplifiers**: Miller effect, CS amplifier, source follower, CG amplifier, cascade stage, differential amplifier, Multistage amplifier.	4
7.	**Feedback**: Feedback topologies, effect of load, modeling input and output ports in feedback circuits	3

8.	**Noise**: Statistical characteristics, types of noise, single stage amplifiers, differential pair, noise bandwidth, impact of feedback on noise.	3
9.	**Operational Amplifiers**: Performance parameters, One-stage and two-stage Op Amps, gain boosting, comparison, common mode feedback, input range, slew rate, power supply rejection, noise in Op Amps	6
10.	**Stability and Frequency Compensation**: Multi pole systems, phase margin, frequency compensation	3
11.	**High Performance CMOS Op-Amp**: Buffered Op-amps, High speed/Frequency Op-amps, Differential output op-amps, low noise and low voltage op-amps	6
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/Authors	Year of Publication
1.	Razavi, B., "Design of Analog CMOS Integrated Circuits", 1st Ed., Mc Graw Hill.	2001
2.	Gray, P.R., Hurst, P. J., Lewis, S.H., Meyer, R.G., "Analysis and Design of Analog Integrated Circuits", 4th Ed., John Wiley and Sons.	2001
3.	Baker, R. J., Li, H. W. and Boyce, D. E., "CMOS Circuit Design ,Layout and Simulation", Prentice-Hall of India.	1998

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–582** Course Title: **Semiconductor Microwave Devices and Applications**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **Nil**

8. Subject Area: **PEC and DEC**

9. Objective: To introduce to the students the principles of operation of various microwave and millimeter wave semiconductor devices and their circuit applications.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	Transient and ac behaviour of p-n junctions, effect of doping profile on the capacitance of p-n junctions, noise in p-n junctions, high-frequency equivalent circuit, varactor diode and its applications; Schottky effect, Schottky barrier diode and its applications; Heterojunctions.	8
2.	Tunneling process in p-n junction and MIS tunnel diodes, V-I characteristics and device performance, backward diode.	3
3.	Impact ionization, IMPATT and other related diodes, small- signal analysis of IMPATT diodes.	4
4.	Two-valley model of compound semiconductors, Vd-E characteristics, Gunn effect, modes of operation, small-signal analysis of Gunn diode, power frequency limit.	4
5.	Construction and operation of microwave PIN diodes, equivalent circuit, PIN diode switches, limiters and modulators.	3
6.	High frequency limitations of BJT, microwave bipolar transistors, heterojunction bipolar transistors; Operating characteristics of MISFETs and MESFETs, short-channel effects, high electron mobility transistor.	7
7.	Characteristics and design of microstrips, slotlines and coplanar waveguides.	3

8.	Design considerations for microwave and millimeter wave amplifiers and oscillators, circuit realization, noise performance.	7
9.	Introduction to MEMS for RF applications: micromachining techniques for fabrication of micro switches, capacitors and inductors.	3
	Total	**42**

11. Suggested Books:

Sl. No.	**Name of Books/Authors**	**Year of Publication**
1.	Sarrafzadeh, M. and Wong, C.K., "An Introduction to VLSI Physical Design", 4th Ed., McGraw-Hill.	1996
2.	Wolf, W., "Modern VLSI Design System on Silicon", 2nd Ed., pearson Education.	2000
3.	Sait, S.M. and Youssef, H "VLSI Physical Design Automation: Theory and practice", World scientific.	1999
4.	Dreschler, R., "Evolutionary Algorithm for VLSI CAD", 3rd Ed., springer	2002
5.	Sherwani, N.A., "Algorithm for VLSI Physical Design Automation", 2nd ED., Kluwer.	1999
6	Lim, S.K., "Practical problems in VLSI physical Design Automation", Springer.	2008

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–583** Course Title: **Optoelectronic Materials and Devices**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **Nil**

8. Subject Area: **PEC and DEC**

9. Objective: To develop understanding of optical materials, working of optoelectronic devices and their applications.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	Optical processes in semiconductors, EHP formation and recombination, absorption and radiation in semiconductor, deep level transitions, Auger recombination, luminescence and time resolved photoluminescence, optical properties of photonic band-gap materials.	7
2.	Junction photodiode: PIN, heterojunction and avalanche photodiode; Comparisons of various photodetectors, measurement techniques for output pulse.	5
3.	Photovoltaic effect, V-I characteristics and spectral response of solar cells, heterojunction and cascaded solar cells, Schottky barrier and thin film solar cells, design of solar cell.	6
4.	Modulated barrier, MS and MSM photodiodes; Wavelength selective detection, coherent detection; Microcavity photodiode.	7
5.	Dynamic effects of MOS capacitor, basic structure and frequency response of charge coupled devices, buried channel charge coupled devices.	5
6.	Electroluminescent process, choice of light emitting diode (LED) material, device configuration and efficiency; LED: Principle of operation, LED structure, frequency response, defects, and reliability.	5

7.	Semiconductor laser diode, Einstein relations and population inversion, lasing condition and gain, junction lasers, hetrojunction laser, multi quantum well lasers, beam quantization and modulation.	7
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/Authors	Year of Publication
1.	Liao, S.Y., "Microwave Devices and Circuits", 4thEd., Pearson Education.	2002
2.	Rebeiz, M.G., "R.F. MEMS: Theory, Design and Technology", 2ndEd., Wiley-Interscience.	2003
3.	Sze, S.M., and Ng, K.K., "Physics of Semiconductor Devices", 3rdEd. Wiley-Interscience.	2006
4.	Glover, I.A., Pennoek, S.R. and Shepherd P.R., "Microwave Devices, Circuits and Sub-Systems", 4th Ed., John Wiley & Sons.	2005
5.	Golio, M., "RF and Microwave Semiconductor Devices Handbook", CRC Press.	2002
6	Zumbahlen, H.(ed.), "Linear Circuit Design Handbook", Elsevier.	2008

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–584** Course Title: **Mixed Signal Circuit Design**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **Analog VLSI Circuit Design, Digital VLSI Circuit Design, MOS Device Physics**

8. Subject Area: **PEC and DEC**

9. Objective: To acquaint students with CMOS mixed signal circuit design.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Signals, Filters and Tools**: Sinusoidal signal, Comb filters and representation of signals	2
2.	**Sampling and Aliasing**: Impulse Sampling, Decimation, K-Path Sampling Sample-and-Hold, Track-and-Hold, Implementation of S/H, Discrete Analog Integrator	3
3.	**Analog Filters**: Integrator building blocks, MOSFET-C Integrator g_m-C Integrators, Discrete time Integrators, Filtering topologies, Bilinear and Biquadratic Transfer function	5
4.	**Digital Filters**: SPICE Models for DACs and ADCs, Sinc Shaped digital filters, Bandpass and Highpass sinc Filters, Filtering topologies, FIR Filter, Concept of stability and Overflow	6
5.	**Data Convertor SNR**: Quantization noise, Signal-to-Noise Ration (SNR), Concept of Spectral Density, Clock Jitter reduction techniques, Improving	6
6.	**Data Convertor Design:** One bit ADC and DAC, Passive Noise shaping, Improving SNR and Linearity, Improving Linearity using Active circuits,	6
7.	**Noise Shaping Data Converters**: First Order Noise Shaping, Second order noise shaping, noise shaping topologies, Cascaded Modulators	4
8.	**Bandpass Data Converters**: Continuos Time bandpass noise shaping, Active and Passive component bandpass modulators, switched capacitor bandpass modulator, Digital I/Q Extraction to bandpass	4

9.	**High Speed Data Converters:** Topologies, path settling time, implementation, generation of clock signals and comparators, Clocked comparators, ADC	6
	Total	**42**

11. Suggested Books:

Sl. No.	**Name of Books/Authors**	**Year of Publication**
1.	Baker Jacob R, "CMOS Mixed signal Circuit Design," Wiley IEEE Press	2009
2.	Baker Jacob R., "CMOS circuit design layout and simulation" Wiley IEEE	2010
3.	Razavi, B., "Design of Analog CMOS Integrated Circuits", 1st Ed., Mc Graw Hill.	2001

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–585** Course Title: **VLSI System Design**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **Digital Electronics, Non-Linear Circuits**

8. Subject Area: **PEC and DEC**

9. Objective: To acquaint students with CMOS mixed signal circuit design.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Introduction to Placement and Routing:** PNR and Routing, Placement Optimisation, Routing Algorithms and its application to simple design issues	4
2.	**Introduction to Static Timing Analysis**: STA with ideal clocks, flip-flop behavior analysis using state diagrams, STA using clock jitters, Example Study for a real chip, Multiple Clock, data transition with respect to power analysis,	6
3.	**Introduction to Clock Tree**: Clock Tree synthesis- H-tree, Buffering, Synthesis timing, set-up analysis with multiple clock,	6
4.	Stack subsystem design, control timing, generation of control signals. Register to Register Transfer. Combinational Logic. The Programmable Logic Array. Basic concept, Circuit design, and stick diagram of example. Finite State Machines,	6
5.	Datapath Operators, Adder, Parity Generator, Comparator ALU, Multiplexer Multiplier, Shifter	6
6.	Design Abstraction, Design Description Language VHDL/VERILOG, Register Transfer Design, Data and Control Flow Representations, Scheduling and Allocation Algorithms, Data and Control Synthesis and Optimization	6

7.	**Layout Generation:** Partitioning, Floor Planning, Placement, Routing –Global, Channel and Switch box Routing, Power and Clock distribution, Pad Design	4
8.	**Memory Units**: Read-Only Memories – ROM Cells Read/Write Memory - SRAM and DRAM Cells, Address Decoder, Sense Amplifier, Programmable Logic Arrays, Application Specific IC Design issues	4
	Total	**42**

11. Suggested Books:

Sl. No.	**Name of Books/Authors**	**Year of Publication**
1.	Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic 'Digital Integrated Circuits: A Design Prespective. Second Edition, A Prentice-Hall Publication Hall, 2003	2003
2.	N.Weste and D.Harris, "CMOS VLSI Design: Circuits and Systems Perspective," Fourth edition, Addison Wesley, 2010	2010

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–586** Course Title: **Device-Circuit Interaction**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester ✓

Autumn **Spring** **Both**

7. Pre-requisite: **EC – 142, EC -104, EC - 201**

8. Subject Area: **PEC and DEC**

9. Objective: To acquaint the students with microelectronics device and circuit interaction issues.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Performance of Circuits using Short-Channel MOSFETs**: Circuit performance considering short channel and narrow width effects, mechanical stress.	8
2.	**Performance of Circuits using Nanoscale MOSFETs**: Quantum confinement of carriers, quasi-ballistic transport and band-to-band tunneling, impact of carrier confinement and quasi-ballistic transport on circuit performance.	8
3.	**FinFETs and GAA Transistors**: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA	12
4.	**Steep Slope Devices**: Tunnel FETs, I-MOS, resonant TFETs, ferroelectric negative capacitance devices, circuits using steep slope devices.	8
5.	**Germanium and III-V Integration in MOSFETs**: Mobility and injection velocity enhancement, hetero-junction issues at source/drain-channel interface, performance of circuits using compound semiconductor devices.	6
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publicatio
1.	Yuan Taur and T. Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press.	1998
2.	Mark Lundstrom and J. Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation," Springer.	2007
3.	J. –P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer.	2009
4.	Selected papers from IEEE, Elsevier and IOP journals.	

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code**: ECN – 587** Course Title**: Nanoscale Devices**

2. Contact Hours: **L: 3 T: 1 P: 0**

3. Examination Duration (Hrs.): **Theory** 0 | 3 **Practical** 0 0

4. Relative Weight**:** **CWS** 15 **PRS** 00 **MTE** 35 **ETE** 50 **PRE** 00

5. Credits**:** 0 | 4 6. Semester √ **Autumn** ☐ **Spring** ☐ **Both**

7. Pre-requisite**: None**

8. Subject Area**: PCC and DEC**

9. Objective: To instigate fundamental concepts of solid state physics and basic semiconductor devices.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Long Channel MOSFETs**: History; Introduction – MOSFET as a barrier controlled device; MOSFET I-V characteristics; Drain current models, MOSFET scaling; subthreshold characteristics; substrate bias and temperature dependence, MOSFET electrostatics – energy band picture, 1D electrostatic Poisson-Boltzmann equation, depletion approximation, onset of inversion, gate voltage and surface potential, static and mobile charges.	5
2.	**Short Channel Effects**: Charge sharing; channel length modulation; DIBL; GIDL; velocity saturation; MOSFET breakdown; concepts of high-K/metal gate;	5
3.	**Advanced planar and 3D transistors**: FDSOI, DG-ETSOI; FINFETs, nanowires.	5
4.	**Nanoscale transport:** Bottom-up approach, Landauer's formalism, Ballistic and diffusive transport – modes, IV characteristics, conductance, voltage drop and heat dissipation, ballistic MOSFET, ballistic injection velocity, Virtual Source Model,	15
5.	**Current topics and open issues**: Strained Si technology, NEGF, Thermoelectric effects and thermoelectric devices, Quantum dot devices – quantum capacitance, IV characteristics, self-consistent method.	12
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publication
1.	Selected Journal and Conference papers	
2.	Mark Lundstorm, “Fundamentals of Nanotransistors,” World Scientific.	2016
3.	Tak H. Ning and Yuan Taur, “Fundamentals of Modern VLSI Devices” Pearson Education India Pvt. Ltd.	2015
4.	Donald A. Neamen, “Semiconductor Physics and Devices”, McGraw Hill Higher Education	2002
5	S. M. Sze and Kwok K. Ng, “Physics of Semiconductor Devices,” Wiley	2008

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–588** Course Title: **Performance and Reliability of VLSI Circuits**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **MOS Device Physics, Digital VLSI Circuit Design, Analog VLSI Circuit Design**

8. Subject Area: **PEC and DEC**

9. Objective: To acquaint the students with state-of-the-art circuit performance and reliability models of VLSI circuits.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Nanoscale MOSFET Characteristics**: Quasi-ballistic I-V characteristics, terminal capacitances of transistors considering quantum effects, parasitic resistances in nanoscale MOSFETs.	5
2.	**Delay and Timing Models:** Classical delay models of logic gates, logic gate delay models for nano-regime CMOS technologies, timing parameters of sequential circuit elements, access-time of CMOS memories, impact of process/temperature/supply-voltage variations on timing parameters.	12
3.	**Power Consumption:** Models for dynamic power, short circuit power and leakage power of CMOS circuits, full-chip power estimation techniques, impact of process/temperature variations on power consumption.	6
4.	**Reliability of CMOS Circuits:** Circuit performance considering NBTI/PBTI, oxide breakdown, random telegraph noise, radiation damage.	11
5.	**Analog Circuit Performance Parameters**: Impact of parasitic effects, process/temperature variation, device reliability effects.	8
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publication
1.	Yuan Taur and T. Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press.	1998
2.	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective," Prentics Hall	2003
3.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw-Hill.	2002
4.	Selected papers from IEEE, Elsevier and IOP journals.	

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–589** Course Title: **Advanced VLSI Interconnects**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **EC – 201, Digital VLSI Circuit Design**
8. Subject Area: **PEC and DEC**

9. Objective: To provide in depth knowledge of interconnect modeling and performance analysis; introduction and analysis of futuristic material based interconnects such GNRs, CNTs and fiber optics.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Preliminary concepts**: Interconnects for VLSI applications, metallic interconnects, optical interconnects, superconducting interconnects, advantages of copper interconnects, challenges posed by copper interconnects, fabrication process, even and odd mode capacitances, miller theorem, transmission line equations, resistive interconnection as ladder network, propagation modes in microstrip interconnection, slow wave mode propagation, propagation delays.	8
2.	**Parasitic extraction:** Parasitic resistance, effect of surface/interface scattering and diffusion barrier on resistance, Capacitance: parallel-plate capacitance, fringing capacitance, coupling capacitance, methods of capacitance extraction, Inductance: self-inductance, mutual inductance, methods of inductance extraction, high frequency losses, frequency dependent parasitics, skin effect, dispersion effect.	8

3.	**Modeling of interconnects and Crosstalk analysis**: Elmore model, Transfer function model, even and odd mode model, Time domain analysis of multiconductor lines, Finite Difference Time Domain (FDTD) method, performance analysis using linear driver (Resistive) and nonlinear driver (CMOS), advanced interconnect techniques to avoid crosstalk.	8
4.	**Future VLSI Interconnects**: Optical interconnects, Superconducting interconnects, Nanotechnology interconnects, Silicon nanowires, Carbon nanotubes, Graphene nanoribbons: system issues and challenges, material processing issues and challenges, design issues and challenges.	9
5.	**Carbon nanotube and Graphene nanoribbon VLSI interconnects:** Quantum electrical properties: quantum conductance, quantum capacitance, kinetic inductance, Carbon nanotube (CNT) and Graphene nanoribbon (GNR) interconnects, electron scattering and lattice vibrations, electron mean free path, single-wall CNT and single layer GNR resistance model, multi-wall CNT and multi-layer GNR resistance model, transmission line interconnect models, performance comparison of CNTs, GNRs and copper interconnects.	9
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publication
1.	High-Speed VLSI Interconnects, Ashok K. Goel	2007
2.	Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications, Y.S. Diamand	2009
3.	Carbon nanotube and Graphene Device Physics, H.S Philip Wong and Deji Akinwande	2011

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–590** Course Title: **Organic Electronics**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **Semiconductors; electronic materials properties, Microelectronics, VLSI circuit**

8. Subject Area: **PEC and DEC**

9. Objective: Study, modeling and simulation of organic material based devices and circuits. Acquaint the students with the conducting polymers, small-molecules, organic materials, different structures of OFETs, OLEDs and various applications of organic thin film transistors.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Organic and Inorganic Materials & Charge Transport:** Introduction; Organic Materials: Conducting Polymers and Small Molecules, Organic Semiconductors: p-type, n-type, Ambipolar Semiconductors, Charge Transport in Organic Semiconductors, Charge Transport Models, Energy Band Diagram, Organic and inorganic materials for: Source, Drain and Gate electrodes	8
2.	**Device Physics and Structures: Organic Thin Film Transistors:** Overview of Organic Field Effect Transistor (OFET); Operating Principle; Classification of Various Structures of OFETs; Output and Transfer Characteristics; OFETs Performance Parameters: Impact of Structural Parameters on OFET; Extraction of Various Performance Parameters, Advantages, Disadvantages and Limitations.	8

3.	**Organic Device Modeling and Fabrication Techniques:** Modeling of OTFT Different Structures, Origin of Contact Resistance, Contact Resistance Extraction, Analysis of OFET Electrical Characteristics, Validation and Comparison of OFETs. Organic Devices and Circuits Fabrication Techniques.	8
4.	**OLEDs and Organic Solar Cells** Organic Light Emitting Diodes (OLEDs): Introduction; Different Organic Materials for OLEDs; Classification of OLEDs, Output and Transfer Characteristics; Various Optical, Electrical and Thermal properties, Advantages, Disadvantages and Limitations. Organic Solar Cells: Introduction, Materials, various properties, Characteristics, Advantages, Disadvantages and Limitations and Applications;	10
5.	**OTFT Applications** Organic Inverters: Inverter Circuits based on Different Materials Combination and Configurations; All-p-type, Organic Complementary Inverter Circuits, Hybrid Complementary Inverters, Comparison between All P-Type, Fully Organic and Hybrid Complementary Inverter Circuits; Logic Circuit Implementation; Organic Memory: Organic Static Random Access Memory (OSRAM) Organic DRAM, Shift registers and other Important Organic Memory Designs. OTFT as Driver for organic Light Emitting Diodes (OLEDs). Addition of More Applications based on Recent Technology Development.	8
	Total	**42**

11. Suggested Books:

SL. No.	Name of Authors/Books/Publishers	Year of Publication/Reprint
	Text Books	
1.	Hagen Klauk, Organic Electronics: Materials, Manufacturing and Applications, Wiley-VCH Verlag Gmbh & Co. KGaA, Germany.	2006
2.	Klaus Mullen, Ullrich Scherf, Organic Light Emitting Devices: Synthesis, Properties and Applications, Wiley-VCH Verlag Gmbh & Co. KGaA, Germany.	2005
	Reference Books	
1.	Hagen Klauk, Organic Electronics II: More Materials and Applications, Wiley-VCH Verlag Gmbh & Co. KGaA, Weinheim, Germany, 2012	2012
2.	Flora Li, Arokia Nathan, Yiliang Wu, Beng S. Ong, Organic Thin Film Transistor Integration: A Hybrid Approach, Wiley-VCH, Germany; 1st Ed.	2011
3.	Wolfgang Brutting, Physics of Organic Semiconductors, Wiley-VCH Verlag Gmbh & Co. KGaA, Germany.	2005
4.	Dresselhaus, M.S., Dresselhaus, G. and Avouris, P., Carbon Nanotubes: Synthesis, Structure, Properties and Applications. New York: Springer- Verlag,	2001

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–591** Course Title: **VLSI Physical Design**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **Digital VLSI Circuit Design**

8. Subject Area: **PEC and DEC**

9. Objective: To develop understanding of state-of-the-art tools and algorithms, which address design tasks such as floor planning, module placement and signal routing for VLSI logic and physical level design

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Introduction:** Layout and design rules, materials for VLSI fabrication, basic algorithmic concepts for physical design, physical design processes and complexities.	2
2.	**Partition:** Kernigham-Lin's algorithm, Fiduccia Mattheyes algorithm, Krishnamurty extension, hMETIS algorithm, multilevel partition techniques.	6
3.	**Floor-Planning:** Hierarchical design, wirelength estimation, slicing and non- slicing floor plan, polar graph representation, operator concept, Stockmeyer algorithm for floor planning, mixed integer linear program.	10
4.	**Placement:** Design types: ASICs, SoC, microprocessor RLM; Placement Techniques: Simulated annealing, partition-based, analytical, and Hall's quadratic; Timing and congestion considerations.	8
5.	**Routing:** Detailed, global and specialized routing, channel ordering, channel Routing problems and constraint graphs, routing algorithms, Yoshimura and Kuh's method, zone scanning and net merging, boundary terminal problem, minimum density spanning forest problem, topological routing, cluster graph representation.	12

6.	**Sequential Logic Optimization and Cell Binding**: State based optimization, state minimization, algorithms; Library binding and its algorithms, concurrent binding	4
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publication
1.	Sarrafzadeh, M. and Wong, C.K., "An Introduction to VLSI Physical Design", 4th Ed., McGraw-Hill.	1996
2.	Wolf, W., "Modern VLSI Design System on Silicon", 2nd Ed., Pearson Education.	2000
3.	Sait, S.M. and Youssef, H., "VLSI Physical Design Automation: Theory and Practice", World Scientific.	1999
4.	Dreschler, R., "Evolutionary Algorithms for VLSI CAD", 3rd Ed., Springer	2002
5.	Sherwani, N.A., "Algorithm for VLSI Physical Design Automation", 2nd Ed., Kluwer.	1999
6.	Lim, S.K., "Practical Problems in VLSI Physical Design Automation", Springer.	2008

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–592** Course Title: **Compound Semiconductors and RF Devices**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **Nil**

8. Subject Area: **PEC and DEC**

9. Objective: To provide knowledge of various compound semiconductor alloys, and their growth, properties, devices and applications.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**III-V opto- and high frequency materials**: Bonds, crytstal lattices, crystallographic planes and directions, direct and indirect semiconductors and their comparison for optical applications, optical processes of absorption and emission , radiative and non-radiative deep level transitions, phase and energy band diagrams of binary, ternary and quaternary alloys, determination of cross-over compositions and band structures.	10
2.	**High frequency devices**: Gunn diode, RWH mechanism, v-E characteristic, formation of domains, modes of operation in resonant circuits, fabrication, control of v-E characteristics by ternary and quaternary alloys.	8
3.	**Heterostructures:** Introduction, abrupt isotype/anisotype junctions, band diagrams and band off-sets, electrical and optoelectronic properties, symmetrical and asymmetrical p-n diodes and their characteristics, 2-Dimensional Electron Gas (2- DEG).	8
4.	**Heterostructure devices**: HBT, MOSFET, HEMT, quantum well and tunneling structures, lasers, LED and photodetectors, optoelectronic IC's and strained layer structures.	8
5.	**Miscellaneous devices**: Compound semiconductor MESFETs, infrared and window effect in photovoltaic converters, strain sensors and their sensitivities, QWITT and DOVETT devices.	8
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Authors / Books / Publishers	Year of Publication /Reprint
1.	Arora, N., "MOSFET Models for VLSI Circuit Simulation: Theory and Practice", 4th Ed., Springer-Verlag.	1993
2.	Tsividis, Y., "Operation and Modeling of the MOS Transistor", 2nd Ed., Oxford University Press.	2003
3.	Sze, S. M., and Ng, K. K., "Physics of Semiconductor Devices", 3rd Ed., Wiley-Interscience.	2006
4.	Liu, W., "MOSFET Models for Spice Simulation (including BSIM3V3 and BSIM4)", Wiley-IEEE Press	2001

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–593** Course Title: **CAD for VLSI**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester ✓

Autumn **Spring** **Both**

7. Pre-requisite: **Digital VLSI Circuit Design, EC - 201**

8. Subject Area: **PEC and DEC**

9. Objective: To provide knowledge on the front end design aspects of VLSI chip manufacturing cycle.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Introduction**: Evolution of design automation; CMOS realizations of basic gates.	3
2.	**Circuit and system representation**: Behavioral, structural and physical models, design flow.	4
3.	**Modeling techniques**: Types of CAD tools, introduction to logic simulation	4
4.	**HDL**: Syntax, hierarchical modeling, Verilog/VHDL construct, simulator directives, instantiating modules, gate level modeling.	6
5.	**Delay modeling**: Event based and level sensitive timing control, memory initialization, conditional compilation, time scales for simulation.	5
6.	**Advanced modeling techniques**: Static timing analysis, delay, switch level modeling, user defined primitive (UDP), memory modeling.	5
7.	**Logic synthesis**: Logic synthesis of HDL construct, technology cell library, design constraints, synthesis of Verilog/VHDL construct.	6
8.	**Model optimization**: Various optimization techniques, design size.	4
9.	**FPGAs based system design**: Commercial FPGA architecture, LUT and routing architecture, FPGA CAD flow; Typical case studies.	5
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publication
1.	Weste, N. and Eshraghian, K., "Principles of CMOS VLSI Design –A Systems Perspective", 2nd Ed., Addison Wesley.	2006
2.	Palnitkar, S., "Verilog HDL", 2nd Ed., Pearson Education.	2004
3.	Wolf, W., "Modern VLSI Design: System on Chip", 2nd Ed., Prentice Hall of India.	2002

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–594** Course Title: **VLSI Digital Signal Processing**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **Digital VLSI Circuit Design**

8. Subject Area: **PEC and DEC**

9. Objective: To provide knowledge on transformations for high speed VLSI digital signal processing using pipelining, retiming, and parallel processing techniques.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Introduction to DSP Systems**: Typical DSP programs, Area-speed-power tradeoffs, Representation methods of DSP systems	2
2.	**Iteration Bound:** Iteration, Iteration period, Iteration bound, Algorithms to compute iteration bound – Longest path matrix, Minimum cycle matrix	4
3.	**Pipelining and Parallel Processing**: Introduction to pipelining and parallel processing, Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power	5
4.	**Retiming**: Retiming formulation, Retiming for clock period minimization, K-slow transformation, Retiming 2-slow graph	4
5.	**Unfolding:** Algorithm for unfolding, Properties of unfolding, Application of unfolding, Sample period reduction, Word and bit-level parallel processing	6
6.	**Folding**: Folding technique, Folding transformation, Retiming for folding	4
7.	**Fast Convolution**: Introduction, Cook-Toom algorithm and modified Cook-Toom algorithm, Winograd algorithm and modified Winograd algorithm, Iterated convolution, Cyclic convolution, Design of Fast convolution algorithm by inspection.	6
8.	**Algorithmic Strength Reduction in Filters and Transforms**: Introduction, Parallel FIR filters, Two-parallel and three-parallel low-complexity FIR filters, 3-parallel fast FIR filter, Parallel filter algorithms	6

	from linear convolutions, Discrete Cosine Transform and Inverse DCT.	
9.	**Pipelined and Parallel Recursive and Adaptive Filters**: Introduction, Pipeling in 1st order IIR digital filters, Pipelining in higher order IIR digital filters, Parallel processing for IIR filters, Combined pipelining and parallel processing for IIR filters.	5
	Total	**42**

11. Suggested Books:

Sl. No.	**Name of Books/ Authors**	**Year of Publication**
1.	Parhi, Keshab K., "VLSI Digital Signal Processing Systems: Design and Implementation", John Willey & Sons.	1999
2.	John G. Proakis, Dimitris Manolakis: Digital Signal Processing: Principles, Algorithms and Applications, 4th ed, Pearson.	2006
3.	Sen M. Kuo, Woon-Seng Gan: Digital Signal Processors: Architectures, Implementations, and Applications, Prentice Hall.	2005

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–595** Course Title: **VLSI Testing & Testability**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester ✓

Autumn **Spring** **Both**

7. Pre-requisite: **Introduction to analog and digital circuits and design, Physical VLSI Design**

8. Subject Area: **PEC and DEC**

9. Objective: Upon completion of this course, students will be able to understand the VLSI chip testing mechanism, systems using existing test methodologies, equipments, and tools.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	Motivation for testing, Design for testability, the problems of digital and analog testing, Design for test, Software testing. **Faults in Digital Circuits**: Controllability, and Observability, Fault models - stuck-at faults, Bridging faults, intermittent faults.	05
2.	**Digital Test Pattern Generation**: Test pattern generation for combinational logic circuits, Manual test pattern generation, Automatic test pattern generation - Roth's D- algorithm, Developments following Roth's D algorithm, Pseudorandom test pattern generation, Test pattern generation for sequential circuits, Exhaustive, non-exhaustive and pseudorandom 70 test pattern Generation, Delay fault testing.	07
3.	**Signatures and Self Test**: Input compression output compression arithmetic, Reed- Muller and spectral coefficients, Arithmetic and Reed-Muller coefficients, Spectral coefficients, Coefficient test signatures, Signature analysis and online self test. Testability Techniques: Partitioning and ad-hoc methods and scan-path testing, Boundary scan and IEEE standard 1149.1, Offline built in Self Test (BIST), Hardware description languages and test.	10
4.	**Testing of Analog and Digital circuits**: Testing techniques for Filters, A/D Converters, Programmable logic devices and DSP, Test generation algorithms for combinational logic circuits – fault table, Boolean difference, Path sensitilization, D- algorithm, Podem, Fault simulation techniques – serial single fault propagation,	12

	Deductive, Parallel and concurrent simulation, Test generation for a sequential logic, Design for testability – adhoc and structured methods, Scan design, Partial scan, Boundary scan, Pseudo-random techniques for test vector generation and response compression, Built–in-Self test, PLA test and DFT.	
5.	**Memory Design and Testing**: Memory Fault Modeling, testing, And Memory Design For Testability And Fault Tolerance RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.	08
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publication
1.	M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory,and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers.	2000
2.	A.K Sharma, Semiconductor Memories Technology, Testing and Reliability, IEEE	

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPT. /CENTRE: **Electronics and Communication Engineering**

1. Subject Code: **ECN–596** Course Title: **MEMS & NEMS**

2. Contact Hours**:** **L: 3** **T: 1** **P: 0**

3. Examination Duration (Hrs.): **Theory 03** **Practical 00**

4. Relative Weight: **CWS 20-35** **PRS 00** **MTE 20-35** **ETE 40-50** **PRE 00**

5. Credits**:** **0 4** 6. Semester **Autumn** ✓ **Spring** **Both**

7. Pre-requisite: **VLSI Technology**

8. Subject Area: **PEC and DEC**

9. Objective: The course will provide understanding of underlying principles of MEMS and NEMS devices, and will provide insight to design related technologies.

10. Details of the Course:

Sl. No.	Contents	Contact Hours
1.	**Introduction to Micro-fabrication**:Cleaning, Oxidation, Diffusion, Mask making, Lithography, Etching, Ion Implantation, CVD, PVD, Metallization; Surface micromachining and Bulk Micromachining, DRIE, LIGA, Fabrication of high aspect ratio deformable structures	8
2.	**Elasticity in Materials**: Stress, strain calculations, Normal and Shear strains and constitutive relations, Plane stress, biaxial stress, residual stress, energy relations, Load-deflection calculations in beams, cantilevers (rectangular cross section), Elastic deformation in square plate, Resonant frequency calculations: Rayleigh-Ritz method	14
3.	**MEMS Capacitive Switch**: Lumped model, pull-in voltage, Electromechanical deflection modeling, pull-in instability, switching time and pull-in voltage scaling, Physical effects in nanoscale gap-size, squeeze-film damping , perforated MEMS Capacitive switch, Comb actuators, Accelerometer, Pressure sensor, Energy approach: Lagrangian Mechanics applicable to MEMS capacitive switches, Reliability in RF-capacitive switch	12
4.	**MEMS Sensors**: Thermal sensor, Interaction of Thermal-Electrical Fields, Numerical design of thermal sensors, Bio-MEMS design problems	4
5.	**Optical MEMS**:2-D, 3-D switches, design examples	4
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publication
1.	Rebeiz, G.M., RF MEMS: Theory Design and Technology,Wiley	1999
2.	Stephen D. Senturia, Microsystem Design, Kluwer Academic	2001
3.	Madou, M., Fundamentals of Microfabrication, CRC Press	1997
4.	Sandana A., Engineering biosensors: kinetics and design applications, Academic Press	2002
5.	Related research papers	

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPARTMENT/CENTRE: Department of Electronics and Communication Engineering

1. **Subject Code:** ECN-524 **Course Title:** Power Electronic Devices, Circuits and systems
2. **Contact Hours:** **L:** 3 **T:** 1 **P:** 0
3. **Examination Duration (Hrs.):** **Theory:** 3 **Practical:** 0
4. **Relative Weightage:** **CWS:** 20-35 **PRS:** 0 **MTE:** 20-30 **ETE:** 40-50 **PRE:** 0
5. **Credits:** 4 **6. Semester:** Spring **7. Subject Area:** PEC
8. **Pre-requisite:** A knowledge of fundamentals of semiconductor device physics
9. **Objective:** To introduce concepts of power electronic semiconductor devices, power conversion circuits and systems.

10. **Details of the Course**

S.No.	Contents	Contact hours
1.	**Introduction**: Evolution of Power Semiconductor Devices; Continuous and Switch Mode Operations; Control Switches; Power Losses; Resistive Inductive and Capacitive Load.	3
2.	**Carrier Transport and Breakdown:** Review of Semiconductor Transport Mechanisms: Drift, Diffusion and Recombination Mechanisms in Power Electronics; Avalanche Breakdown: Impact Ionization Integral and Multiplication Coefficients; Edge-Termination Techniques.	7
3.	**Power Semiconductor Devices**: P-N Junction Diode; Fast Recovery Diode; Schottky Diodes; Silicon Controlled Rectifier (SCR); Triode; Bipolar Junction Transistors (BJTs); MOSFETs; Insulated Gate Bipolar Transistors (IGBTs); Baliga Figure of Merit (BFOM); Freewheeling and Flyback Diodes.	10
4.	**Passive Components**: Theory of Inductors and Capacitors, Active and Passive Filters, Design of Inductors in Power Electronics.	4
5.	**Power circuits:** Single-phase and Three-phase Rectifiers, AC-AC Converters, Isolated and Non-isolated DC-DC converters, Inverters, Half-Bridge Converter, Other Power Circuits From Recent Literature, Simulation of Selected Circuits in MATLAB or SPICE.	10
6.	**Control Circuitry for Power Electronics:** Gate Drive Circuits, Snubber Circuit, Pulse-Width Modulation, Basics of PID Controller, Sensing Circuitry, Integrated Power Electronic Systems, Hybrid Integration.	8
Total		**42**

11. **Suggested Books:**

S.No.	Name of Authors/Book/Publisher	Year of Publication / Reprint
1.	B. Jayant Baliga, “Fundamentals of Power Semiconductor Devices (second edition),” Springer.	2019
2.	J. Lutz, H. Schlangenotto, U. Scheuermann and R. D. Doncker “Semiconductor Power Devices Physics, Characteristics, Reliability (second edition),” Springer.	2018

3.	Daniel W. Hart, “Power Electronics,” McGraw Hill Companies Inc.	2011
4.	Issa Batarseh and Ahmad Harb, “Power Electronics Circuit Analysis and Design,” Springer	2018
5.	Frede Blaabjerg, “Control of Power Electronic Converters and Systems,” Academic Press, Elsevier Inc.	2018
6.	Stefanos Manias, “Power Electronics and Motor Drive Systems,” Academic Press, Elsevier Inc.	2016
7.	Liuping Wang, Shan Chai, Dae Yoo, Lu Gan and Ki Ng, “PID and Predictive Control of Electrical Drives and Power Converters using Matlab/Simulink,” John Wiley & Sons Singapore Pte. Ltd	2014
8.	Hebertt Sira-Ramirez and Ramón Silva-Ortigoza, “Control Design Techniques in Power Electronics Devices,” Springer	2006

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPARTMENT/CENTRE: Department of Electronics and Communication Engineering

1. **Subject Code:** ECN-526 **Course Title:** Statistical Machine Learning for Variation-Aware Electronic Device and Circuit Simulation
2. **Contact Hours:** **L:** 3 **T:** 1 **P:** 0
3. **Examination Duration (Hrs.):** **Theory:** 3 **Practical:** 0
4. **Relative Weightage:** **CWS:** 20-35 **PRS:** 0 **MTE:** 20-30 **ETE:** 40-50 **PRE:** 0
5. **Credits:** 4 **6. Semester:** Spring **7. Subject Area:** PEC
8. **Pre-requisite:** Knowledge of basic concepts in probability and statistics
9. **Objective:** To familiarize students with the fundamental concepts, techniques and algorithms needed to perform stochastic simulation and uncertainty quantification of electronic devices, circuits and systems.

10. Details of the Course

S.No.	Contents	Contact hours
1.	**Introduction**: Introduction to stochastic modeling of general systems, key differences between stochastic simulation and classical deterministic simulation. The need for uncertainty quantification in general device, circuit, and system simulation.	**2**
2.	**Introduction to Random Variables:** Discrete and continuous random variables: distribution and density functions, conditional distributions and expectations, functions of random variables, statistical moments, sequence of random variables, central limit theorem, Gaussian and non-Gaussian correlation among random variables	**3**
3.	**Random Sampling Techniques**: Utilization of random sampling techniques for statistical analysis such as Monte Carlo, quasi-Monte Carlo, Latin hypercube sampling, analysis of computational complexity and convergence rate of different random sampling techniques	**5**
4.	**Statistical Machine Learning - Generalized Polynomial Chaos (PC) Theory**: Basic foundation of polynomial chaos, generalization of polynomial chaos for different known distributions, Wiener-Askey scheme of polynomials, generation of orthonormal basis functions using three-term recurrence series and Gram-Schmidt algorithm, training of polynomial chaos metamodels using quadrature techniques and least-squares linear regression. Deployment of PC theory for calculating statistical moments and density functions in linear and nonlinear VLSI as well as RF/microwave devices, circuits, and systems via test cases and illustrative examples.	**6**
5.	**Correlations in PC Theory:** Considering uncorrelated, Gaussian correlated, and non-Gaussian (mixed Gaussian model) correlated parametric variations.	**5**
6.	**Advanced PC theory:** Complexity analysis of PC theory and techniques: limitations of curse of dimensionality in PC theory, emphasis on sensitivity analysis-based dimension reduction, active subspaces, sliced inverse	**13**

	regression, compressed sensing, partial least-squares algorithm, and multi-fidelity methods.	
7.	**Inverse Problems:** Bayes rule, Bayesian formulation of inverse problems, prior and posterior distributions, calculation of maximum likelihood function using PC theory. Applications into inverse uncertainty quantification in linear/nonlinear devices, circuits and systems	**8**
Total		**42**

11. Suggested Books:

S.No.	Name of Authors/Book/Publisher	Year of Publication / Reprint
1.	D. Xiu, "Numerical Methods for Stochastic Computations: A Spectral Method Approach," New Jersey: Princeton University Press	2010
2.	D. Dubois and H. Prade, "Possibility Theory: An Approach to Computerized Processing of Uncertainty," vol. 2, New York, NY: Plenum Press	1988
3.	K. C. Gupta and Q. J. Zhang, "Neural Networks for RF and Microwave Design," Arctech House	2000
4.	A. Papoulis and S. Pillai, "Probability, Random Variables and Stochastic 2017 Processes", 4th Edn., Mc Graw Hill.	2017
5.	R. Shen, S. X.-D. Tan, and H. Yu, Statistical Performance Analysis and Modeling of Nanometer VLSI. New York, NY: Springer	2012

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPARTMENT/CENTRE: Department of Electronics and Communication Engineering

1. **Subject Code:** ECN-525 **Course Title:** Hardware Architecture for Deep-Learning
2. **Contact Hours:** **L:** 3 **T:** 1 **P:** 0
3. **Examination Duration (Hrs.):** **Theory:** 3 **Practical:** 0
4. **Relative Weightage:** **CWS:** 20-35 **PRS:** 0 **MTE:** 20-30 **ETE:** 40-50 **PRE:** 0
5. **Credits:** 4 **6. Semester:** Both **7. Subject Area:** PEC
8. **Pre-requisite:** None
9. **Objective:** To learn the design of hardware architectures and accelerators for deep-learning/artificial-intelligence. This course is at the intersection of deep-learning and computer-architecture/embedded-system/VLSI.

10. Details of the Course

S.No.	Contents	Contact hours
1.	**Background topics:** Approximate computing and storage, Roofline Model, Cache tiling (blocking), GPU architecture, CUDA programming, understanding GPU memory hierarchy, FPGA architecture, Matrix multiplication using systolic array	8
2.	**Convolutional strategies:** Direct, FFT-based, Winograd-based and Matrix-multiplication based.	3
3.	**Deep Learning on various hardware platforms:** Deep learning on FPGAs and case study of Microsoft's Brainwave, Deep learning on Embedded System (especially NVIDIA's Jetson Platform), Deep learning on Edge Devices (smartphones), Deep learning on an ASIC (especially Google's Tensor Processing Unit.), Deep-learning on CPUs and manycore processor (e.g., Xeon Phi), Memristor-based processing-in-memory accelerators for deep-learning.	15
4.	Model-size aware Pruning of DNNs, Hardware architecture-aware pruning of DNNs, Understanding soft-errors. Understanding reliability of deep learning algorithms and accelerators	6
5.	Comparison of memory technologies (SRAM, DRAM, eDRAM, STT-RAM, PCM, Flash) and their suitability for designing memory-elements in DNN accelerator, Neural branch predictors and their applications	4
6.	Hardware/system-challenges in autonomous driving, Distributed training of DNNs and addressing memory challenges in DNN training	6
Total		**42**

11. Suggested Books:

S.No.	Name of Authors/Book/Publisher	Year of Publication / Reprint
1.	**Computer Architecture: A quantitative approach** (Sixth Edition), Hennessy, J. L., & Patterson, D. A., Elsevier https://www.google.co.in/books/edition/Computer_Architecture/cM8mDwAAQBAJ	2017

2.	**Deep Learning for Computer Architects** Brandon Reagen, Robert Adolf, Paul Whatmough, Gu-Yeon Wei, and David Brooks Synthesis Lectures on Computer Architecture, August 2017, Vol. 12, No. 4, Pages 1-123 (https://doi.org/10.2200/S00783ED1V01Y201706CAC041)	2017
3.	**General-Purpose Graphics Processor Architectures** Tor M. Aamodt, Wilson Wai Lun Fung, and Timothy G. Rogers, Synthesis Lectures on Computer Architecture, May 2018, Vol. 13, No. 2, Pages 1-140 (https://doi.org/10.2200/S00848ED1V01Y201804CAC044)	2018
4.	Goodfellow, I., Bengio, Y., Courville, A., & Bengio, Y. (2016). **Deep learning (Vol. 1, No. 2)**. Cambridge: MIT press.	2016
5.	Selected research papers	

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPARTMENT/CENTRE: Department of Electronics and Communication Engineering

1. **Subject Code:** ECN-634 **Course Title**: Low Voltage CMOS Circuit Operation
2. **Contact Hours:** **L:** 3 **T:** 1 **P:** 0
3. **Examination Duration (Hrs.):** **Theory:** 3 **Practical:** 0
4. **Relative Weightage:** **CWS:** 20-35 **PRS:** 0 **MTE:** 20-30 **ETE:** 40-50 **PRE:** 0
5. **Credits:** 4 **6. Semester:** Both **7. Subject Area:** PEC
8. **Pre-requisite:** Knowledge of digital and analog VLSI circuit design/analysis, MOS device physics.
9. **Objective:** To understand essential aspects of low voltage operation of MOSFETs and CMOS circuits comprehensively and to learn to design such circuits.
10. **Details of the Course**

S.No.	Contents	Contact hours
1.	Metrics for evaluating application performance, evaluating, and summarizing performance, energy management approaches (e.g., DVFS).	1
2.	MOSFET operation in weak inversion: Inversion/depletion charge, I-V characteristics, C-V characteristics and device capacitances, short channel effects. 1/f/white/flicker noise.	10
3.	Near-threshold digital CMOS circuits: Transistor sizing in combinational and sequential circuits, warning flip-flops, CMOS memory design and noise margins, dynamic circuits, resilient circuits, PVT variations	8
4.	Low voltage analog circuits: Building blocks of OPAMP, OPAMP design, voltage/current references, switched capacitor circuits. Coping with PVT variations. Noise in circuits.	8
5.	Low voltage mixed-signal circuits: Building blocks for PLLs, PLLs, building blocks for ADCs, ADCs, filters.	9
6.	FinFETs: I-V/C-V in weak inversion, device capacitances, noise, digital, analog circuits.	6
Total		**42**

11. Suggested Books:

S.No.	Name of Authors/Book/Publisher	Year of Publication / Reprint
1.	Sub-Threshold Design for Ultra Low-Power Systems, A. Wang, B. H. Calhoun, and A. P. Chandrakashan, Springer	2006
2.	Low voltage CMOS VLSI Circuits, by J. B. Kuo and J.H Lou, Wiley	1999
3.	Charge-based MOS transistor Modelling The EKV Model for Low-Power and RF IC Design By C.C. Enz and E.A. Vittoz, Wiley	2006
4.	Design of Low-Voltage CMOS switched-Opamp switched-capacitor Systems by V.S.L. Cheung and H.C. Luong, Kluwer Academic Publishers	2003
5.	Low Voltage CMOS Operational Amplifiers (Theory, Design, and Implementation) by S. Sakurai and M. Ismail, Springer	1995
6.	Digital Integrated Circuits, A Design Prospective by J.M. Rabaey, Prentice Hall	2002
7.	Circuit Techniques for Low-voltage and high-speed A/D converters by M.E. Waltari and K.A.I. Halonen, Kluwer Academic Publishers	2002
8.	CMOS Mixed Signal Circuit Design by R.J. Baker, Wiley	2003
9.	Analog Integrated Circuit Design by Tony Chan Carusone, David A. Johns and Kenneth W. Martin, Wiley	2011