Bulusu Anand

Professor

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# Education

* Jan 1999 – Dec 2006: **Ph. D,** Electrical Engineering, Indian Institute of Technology, Bombay
* July 1996-Jan 1998: **M. E** Electrical Engineering (Microelectronics), Birla Institute of Technology and Science, Pilani
* July 1991 – July 1995: **B. E,** Electronics and Communication Engineering, Andhra University, Visakhapatnam

# Current Research Interests:

* Novel device/circuit co-design methodologies
* Variation aware VLSI circuit design methodology
* Delay and timing models for VLSI circuits
* CMOS VCO Design and Modeling
* Near threshold VLSI circuit design

# Professional Background:

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| **From** | **To** | **Designation** | **Organisation** |
| 2006 | 2007 | Sr. Research Engineer | IIT Bombay |
| 2007 | 2008 | Sr. Design Engineeer | Freescale Semiconductor India (Earstwhile Semiconductor Division of Motorola Inc.) |
| 2008 | 2014 | Assistant Professor | IIT Roorkee |
|  2014 | 2019 | Associate Professor | IIT Roorkee |
|  2019 | Present | Professor | IIT Roorkee |

**Publications:**

## IPs:

* 1. Bulusu Anand, Sudeb Dasgupta,Lomash Chandra Acharya, Ajoy Mandal, Venkatraman ramakrishnan,”SAFE :Switching Activity Factor based ECSM characterization methodology for path level timing performance of digital circuits”, Applying for US patent through SRC, Nov 2022.
	2. Bulusu Anand, Shivananda Reddy, Surya Veeraraghavan, “A Method to Find Sensitivity of Standard Cells to Process/Model Changes,” Defensive Publication of Freescale Semiconductor Inc., June 2008, <http://www.priorartdatabase.com/IPCOM/000172383/>
	3. S. K. Manhas, S. Nema, A. Bulusu, “A method of fabricating dual/asymmetric dielectric constant (dual-K) spacers in MOSFET,” Indian Patent No. 406675, 2022.

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## Selected Publications in International Journals:

1. Lomash Chandra Acharya, Arvind Kumar Sharma, Neeraj Mishra, Khoirom Johnson Singh, Mahipal Dargupally, Nayakanti Sai Shabarish, Ajoy Mandal, Venkatraman Ramakrishnan, Sudeb Dasgupta, Anand Bulusu "Aging Aware Timing Model of CMOS Inverter: Path Level Timing Performance and Its Impact on the Logical Effort," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, doi: 10.1109/TCAD.2022.3231173.
2. Neeraj Mishra, Anchit Proch, Lomash Chandra Acharya, Jeffrey Prinzie, Sudipto Chakraborty, Rajiv Joshi, Sudeb Dasgupta, Anand Bulusu *et al*., "Phase Noise Analysis of Separately Driven Ring Oscillators," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022, doi: 10.1109/TCSI.2022.3196820.
3. Khoirom Johnson Singh, Anand Bulusu, Sudeb Dasgupta.Understanding negative capacitance physical mechanism in organic ferroelectric capacitor Solid-State Electronics Vol 194 Pages 108350 August 2022.
4. Sarita Yadav, Nitanshu Chauhan, Raghav Chawla, Arvind Sharma, Shashank Banchhor, Rajendra Pratap, Bulusu Anand.Through-silicon-via induced stress-aware FinFET buffer sizing in 3D ICs Vol 37 Pages 085023 July 2022.
5. K. J. Singh, N. Chauhan, A. Bulusu and S. Dasgupta, "Physical Cause and Impact of Negative Capacitance Effect in Ferroelectric P(VDF-TrFE) Gate Stack and Its Application to Landau Transistor," in *IEEE Open Journal of Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 2, pp. 55-64, 2022, doi: 10.1109/OJUFFC.2022.3172665.
6. Dinesh Kushwaha, Ashish Joshi, Chaudhry Indra Kumar, Neha Gupta, Sandeep Miryala, Rajiv V Joshi, Sudeb Dasgupta, Anand Bulusu *et al*., "An Energy-Efficient High CSNR XNOR and Accumulation Scheme for BNN," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 4, pp. 2311-2315, April 2022, doi: 10.1109/TCSII.2022.3149818.
7. K. J. Singh, A. Bulusu and S. Dasgupta, "Origin of Negative Capacitance Transient in Ultrascaled Multidomain Metal-Ferroelectric-Metal Stack and Hysteresis-Free Landau Transistor," in *IEEE Transactions on Electron Devices*, vol. 69, no. 3, pp. 1284-1292, March 2022, doi: 10.1109/TED.2021.3139057.
8. Nitanshu Chauhan, Navjeet Bagga, Shashank Banchhor, Chirag Garg, Arvind Sharma, Arnab Datta, S Dasgupta, Anand Bulusu.BOX engineering to mitigate negative differential resistance in MFIS negative capacitance FDSOI FET: an analog perspective Nanotechnology Vol 33 Page 085203 December 2021.
9. Sarita Yadav, Nitanshu Chauhan, Shobhit Tyagi, Arvind Sharma, Shashank Banchhor, Rajiv Joshi, Rajendra Pratap, Anand Bulusu.A physical insight into variation aware minimum V DD for deep subthreshold operation of FinFET.Semiconductor Science and Technology Vol 36 Pages 125002October 2021.
10. N. Chauhan, N. Bagga, S. Banchhor, A. Datta, S. Dasgupta and A. Bulusu, "Negative-to-Positive Differential Resistance Transition in Ferroelectric FET: Physical Insight and Utilization in Analog Circuits," in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 69, no. 1, pp. 430-437, Jan. 2022, doi: 10.1109/TUFFC.2021.3116897.
11. C. Garg, N. Chauhan, A. Sharma, S. Banchhor, A. Doneria, S. Dasgupta, A. Bulusu, "Investigation of Trap-Induced Performance Degradation and Restriction on Higher Ferroelectric Thickness in Negative Capacitance FDSOI FET," in *IEEE Transactions on Electron Devices*, vol. 68, no. 10, pp. 5298-5304, Oct. 2021, doi: 10.1109/TED.2021.3105952.
12. L. M. Dani, N. Mishra and B. Anand, "A Variation Aware Jitter Estimation Methodology in ROs Considering Over/Undershoots in NTV Regime," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 3, pp. 1557-1561, March 2022, doi: 10.1109/TCSII.2021.3106796.
13. C. Garg, N. Chauhan, S. Deng, A. I. Khan, S. Dasgupta, Anand Bulusu, Kai Ni, "Impact of Random Spatial Fluctuation in Non-Uniform Crystalline Phases on the Device Variation of Ferroelectric FET," in *IEEE Electron Device Letters*, vol. 42, no. 8, pp. 1160-1163, Aug. 2021, doi: 10.1109/LED.2021.3087335.
14. N. Mishra, L. M. Dani, S. Chakraborty, R. V. Joshi and A. Bulusu, "Delay Modulation in Separately Driven Delay Cells Utilized for the Generation of High-Performance Multiphase Signals Using ROs," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 1, pp. 30-34, Jan. 2022, doi: 10.1109/TCSII.2021.3081829.
15. Shashank Banchhor, Nitanshu Chauhan, Bulusu Anand.A new physical insight into the zero-temperature coefficient with self-heating in silicon-on-insulator fin field-effect transistors Semiconductor Science and Technology Vol 36 Page 035005 . January 2021
16. L. M. Dani, N. Mishra and A. Bulusu, "An Efficient and Accurate Variation-Aware Design Methodology for Near-Threshold MOS-Varactor-Based VCO Architectures," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 40, no. 10, pp. 2117-2127, Oct. 2021, doi:10.1109/TCAD.2020.3037881.*
17. K. J. Singh, A. Bulusu and S. Dasgupta, "Multidomain Negative Capacitance Effect in P(VDF-TrFE) Ferroelectric Capacitor and Passive Voltage Amplification," in *IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4696-4700, Nov. 2020, doi: 10.1109/TED.2020.3022745.*
18. N. Mishra, L. M. Dani, K. Sanvaniya, S. Dasgupta, S. Chakraborty and A. Bulusu, "Design and Realization of High-Speed Low-Noise Multi-Loop Skew-Based ROs Optimized for Even/Odd Multi-Phase Signals," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 11, pp. 2352-2356, Nov. 2020, doi: 10.1109/TCSII.2019.2959573.
19. Chaudhry I. Kumar and Bulusu Anand, "A Highly Reliable and Energy Efficient Radiation Hardened 12T SRAM Cell Design, Accepted for pubilcation in IEEE Transactions on Device and Material Reliability.
20. Lalit Dani, N. Mishra, A. Sharma, Bulusu Anand, “Variation Aware Prediction of Circuit Performance in Near-threshold Regime using Supply Independent Transition Threshold Points,” IEEE Transactions on Electron Devices, December, 2019.
21. C. I. Kumar and B. Anand, "A Highly Reliable and Energy-Efficient Triple-Node-Upset-Tolerant Latch Design," in *IEEE Transactions on Nuclear Science*, vol. 66, no. 10, pp. 2196-2206, Oct. 2019, doi: 10.1109/TNS.2019.2939380.
22. A. Acharya, A. B. Solanki, S. Glass, Q. T. Zhao and B. Anand, "Impact of Gate–Source Overlap on the Device/Circuit Analog Performance of Line TFETs," in *IEEE Transactions on Electron Devices*, vol. 66, no. 9, pp. 4081-4086, Sept. 2019, doi: 10.1109/TED.2019.2927001.
23. S. Banchhor, K. D. Kumar, A. Dwivedi and B. Anand, "A New Aspect of Saturation Phenomenon in FinFETs and Its Implication on Analog Circuits," in *IEEE Transactions on Electron Devices*, vol. 66, no. 7, pp. 2863-2868, July 2019, doi: 10.1109/TED.2019.2914867.
24. C. I. Kumar, I. Bhatia, A. K. Sharma, D. Sehgal, H. S. Jatana and A. Bulusu, "A Physics-Based Variability-Aware Methodology to Estimate Critical Charge for Near-Threshold Voltage Latches," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 9, pp. 2170-2179, Sept. 2019, doi: 10.1109/TVLSI.2019.2910825.
25. Chaudhry Indra Kumar, Anand Bulusu High performance energy efficient radiation hardened latch for low voltage applications ” Elsevier Integration Journal pp. 119-127 May 2019
26. Chaudhry Indra Kumar, Arvind Kumar Sharma, RajendraPartap, Anand Bulusu, “An energy-efficient variation aware self-correcting latch,” Elsevier Microelectronics Journal, pp. 67 – 78, to be published in February 2019.
27. Chaudhry Indra Kumar and Bulusu Anand, “Design of highly reliable energy-efficient SEU tolerant 10T SRAM cell,” IET Electronics Letters, pp. 1423 – 1424, December 2018.
28. Arvind Sharma, Naushad Alam and Anand Bulusu, “Effective Drive Current for

Near-Threshold CMOS Circuits’ Performance Evaluation: Modeling to Circuit Design Techniques,” IEEE Transactions on Electron Devices, pp. 2413 – 2421, June 2018.

1. Abhishek Acharya, Abhishek Solanki, Sudeb Dasgupta and Bulusu Anand, “Drain Current Saturation in Line Tunneling-Based TFETs: An Analog Design Perspective,” IEEE Transactions on Electron Devices, Volume: 65, Issue: 1, Jan. 2018.
2. Om Prakash , Satish Maheshwaram, Mohit Sharma Anand Bulusu , Sanjeev K. Manhas, “Performance and Variability Analysis of SiNW 6T-SRAM Cell using Compact Model with Parasitics,” IEEE Transactions on Nanotechnology , Volume: 16, Issue: 6, Nov. 2017.
3. Arvind Sharma, Naushad Alam and Anand Bulusu, “Effective Current Model for Inverter-Transmission Gate Structure and Its Application in Circuit Design,” IEEE Transactions on Electron Devices, October 2017.
4. Om Prakash, Swen Beniwal, Satish Maheshwaram, Anand Bulusu, Navab Singh, and S. K. Manhas, “Compact NBTI reliability modeling in Si nanowire MOSFETs and effect in circuits,” IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, VOL. 17, NO. 2, JUNE 2017.
5. Abhishek Acharya, S. Dasgupta, Bulusu Anand, “A Novel VDSAT Extraction Method forTunnel FETs and its Implication on Analog Design” IEEE Transactions on Electron Devices, February 2017.
6. Arvind Sharma, Naushad Alam, Sudeb Dasgupta, Bulusu Anand, “Multifinger MOSFETs’ Optimization Considering Stress and INWE in Static CMOS Circuits”, IEEE Transactions on Electron Devices, PP, no. 99, 2016.
7. Baljit Kaur, Arvind Sharma, Naushad Alam, Sanjeev K. Manhas, Bulusu Anand, “A Variation Aware Timing Model for a 2-Input NAND Gate and Its Use in Sub-65nm CMOS Standard Cell Characterization”, Microelectronics Journal (Elsevier), vol. 53, pp. 45-55, 2016.
8. Archana Pandey; Harsh Kumar; S. K. Manhas; Sudeb Dasgupta; Bulusu Anand, “Atypical Voltage Transitions in FinFET Multistage Circuits: Origin and significance”, IEEE Transactions on Electron Devices, pp. 1392-1396, march 2016.
9. Baljit Kaur, Naushad Alam, S. K. Manhas, Bulusu Anand, “Efficient ECSM characterization considering voltage, temperature and mechanical stress variability,” IEEE Transactions on Circuits and Systems – I, pp. 3407-3415, December 2014.
10. Gaurav Kaushal, S. K. Manhas, S. Maheshwaram, S. Dasgupta, B. Anand, and N. Singh, “Novel Design Methodology Using Lext Sizing in Nanowire CMOS Logic” IEEE Transactions on Nanotechnology, pp. 650-658, July 2014.
11. Naushad Alam, Bulusu Anand and Sudeb Dasgupta, “ An Analytical Delay Model for Mechanical Stress Induced Systematic Variability Analysis in Nanoscale Circuit Design,” IEEE Transactions on Circuits and Systems – I, pp. 1714-1726, June 2014.
12. Archana Pandey, Bulusu Anand, Swati Raycha, Satish Maheshwaram, S. K. Manhas, S. Dasgupta, “Effect of Load Capacitance and Input Transition Time on Underlap FinFET Capacitance,” IEEE Transactions on Electron Devices, pp. 30-36, January 2014.
13. Ashwani Kumar, Vishvendra Kumar, Bulusu Anand, S. Manhas, “Nitrogen-Terminated Semiconducting Zigzag GNR FET With Negative Differential Resistance,” IEEE Transactions on Nanotechnology, pp. 16-22, January 2014.
14. S. Maheshwaram, S. K. Manhas, G. Kaushal, B. Anand and N. Singh, “Vertical Nanowire CMOS Parasitic Modeling and its Performance Analysis,” IEEE Transactions on Electron Devices, vol. 60, no. 9, pp. 2943-2950, Sept. 2013.
15. Menka, Bulusu Anand and Dasgupta S., “Two Dimensional Analytical Modeling for Asymmetric 3T and 4T Double Gate Tunnel FET in Subthreshold Region: Potential and Electric Field”, Microelectronics Journal (In press).
16. N. Alam, B. Anand, and S. Dasgupta, “The Impact of Process-Induced Mechanical Stress in Narrow Width Devices and Variable Taper CMOS Buffer Design", Elsevier Microelectronics Reliability, vol. 53, Issue 5, pp. 718-724, May 2013.
17. N. Alam, B. Anand, and S. Dasgupta, “The Impact of Process-Induced Mechanical Stress on CMOS Buffer Design using Multi-Fingered Devices", Elsevier Microelectronics Reliability, vol. 53, Issue 3, pp. 379-385, March 2013.
18. N. Alam, B. Anand, and S. Dasgupta, "Gate-Pitch Optimization for Circuit Design using Strain-Engineered Multi-Finger Gate Structures", *IEEE Transactions on Electron Devices*, vol. 59, no. 11, pp. 3120-3123, November 2012.
19. Gaurav Kaushal, S. Manhas, S. Maheshwaram, S. Dasgupta, A. Bulusu and N. Singh, “Tuning source/drain extension profile in current matching in nanowire CMOS logic,” IEEE Transactions in Nanotechnology, vol. 11, no. 5, pp. 1033-1035, September 2012.
20. Satish Maheshwaram, S. K. Manhas, G. Kaushal, B. Anand and N. Singh, "Device Circuit Co-Design Issues in Vertical Nanowire CMOS Platform," IEEE Electron Device Letters*,* vol.33, no. 7, pp.934-936, July 2012.
21. Satish Maheshwaram, S. K. Manhas, Gaurav Kaushal, Bulusu Anand, and NavabSingh, “Vertical Silicon Nanowire Gate-All-Around Field Effect Transistor Based Nanoscale CMOS,” IEEE Electron Device Letters, pp. 1011-1013, August 2011.
22. Pradeep Kumar Chawda, B. Anand, V. Ramgopal Rao, “Optimum Body Bias constraints for leakage reduction in high-K Complementary Metal Oxide Semiconductor Circuits,” Japanese Journal of Applied Physics (JJAP), May 2009.
23. Bulusu Anand, M. P. Desai, and V. Ramgopal Rao, "Silicon Film Thickness Optimization for SOI-DTMOS from Circuit Performance considerations", IEEE Electron Device Letters, pp. 436-438, June 2004.
24. P. Sivaram, B. Anand, M. P. Desai, “Silicon film thickness considerations for SOI-DTMOS,” IEEE Electron Device Letters, pp. 276-278, May 2002.

## Selected Publications in International Conferences:

1. Dinesh Kushwaha, Ashish joshi, Neha gupta, aditya sharma, Sandeep miryala, Rajiv Joshi, Sudeb Dasgupta and Anand bulusu “An Energy -Efficient Multi-bit current-based Analog Compute in Memory Architecture and Design Methodology,” VLSI Design Conference, January 2023, Hyderabad.
2. Ashutosh Yadav, Anand Bulusu, Surinder Singh, Sudeb Dasgupta, “Radiation Hardened CMOS Programmable Bias Generator for Space Applications at 180nm,” VLSI Design Conference, January 2023, Hyderabad.
3. Jyoti Patel, Shashank Banchhor, Surila Guglani, Avirup Dasgupta, Sourajeet Roy, Anand Bulusu, Sudeb Dasgupta *et al*., "Design optimization Using Symmetric/Asymmetric Spacer for 14 nm Multi-Fin Tri-gate Fin- FET for Mid-Band 5G Applications," *2022 35th International Conference on VLSI Design and 2022 21st International Conference on Embedded Systems (VLSID)*, 2022, pp. 292-296, doi: 10.1109/VLSID2022.2022.00063.
4. B. S. Prakash, A. Yadav, A. Bulusu and S. Dasgupta, "A Novel High RSNM RHBD 16T SRAM Cell at 180nm," *2021 IEEE 18th India Council International Conference (INDICON)*, 2021, pp. 1-5, doi: 10.1109/INDICON52576.2021.9691597.
5. Neha Gupta, Ashish Joshi, Dinesh Kushwaha, Vinod Menezes, Rashmi Sachan, Sudeb Dasgupta, Anand Bulusu "A Multibit MAC Scheme using Switched Capacitor based 3C Multiplier for Analog Compute In-Memory Architecture," 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2022, pp. 1-4, doi: 10.1109/ICECS202256217.2022.9970819.
6. A. Yadav, A. Bulusu, S. Dasgupta and S. Singh, "Design and Fabrication of Rad-hard Low Power CMOS Temperature Sensor for Space Applications at 180nm," *2021 International Conference on Microelectronics (ICM), 2021, pp. 166-169, doi: 10.1109/ICM52667.2021.9664963.*
7. S. Yadav, N. Chauhan, A. Pandey, R. Pratap and A. Bulusu, "Behaviour of FinFET Inverter’s Effective Capacitances in Low-Voltage Domain," *2021 25th International Symposium on VLSI Design and Test (VDAT), 2021, pp. 1-5, doi: 10.1109/VDAT53777.2021.9601052.*
8. K. J. Singh, A. Bulusu and S. Dasgupta, "Harnessing Maximum Negative Capacitance Signature Voltage Window in P(VDF-TrFE) Gate Stack," *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2021, pp. 1-5, doi: 10.1109/ISCAS51556.2021.9401100.
9. K. J. Singh, A. Bulusu and S. Dasgupta, "Ultrascaled Multidomain P(VDF-TrFE) Organic Ferroelectric Gate Stack to the Rescue," *2021 IEEE Latin America Electron Devices Conference (LAEDC)*, 2021, pp. 1-4, doi: 10.1109/LAEDC51812.2021.9437926.
10. S. Banchhor, N. Chauhan, A. Doneria and B. Anand, "Gain Stabilization Methodology for FinFET Amplifiers Considering Self-Heating Effect," *2021 34th International Conference on VLSI Design and 2021 20th International Conference on Embedded Systems (VLSID)*, 2021, pp. 199-203, doi: 10.1109/VLSID51830.2021.00039.
11. N. Bagga, N. Chauhan, A. Bulusu and S. Dasgupta, "Demonstration of a Novel Ferroelectric-Dielectric Negative Capacitance Tunnel FET," *2019 IEEE Conference on Modeling of Systems Circuits and Devices (MOS-AK India), 2019, pp. 102-105, doi: 10.1109/MOS-AK.2019.8902381.*
12. N. Chauhan et al., "Impact of Random Spatial Fluctuation in Non-Uniform Crystalline Phases on Multidomain MFIM Capacitor and Negative Capacitance FDSOI," 2022 IEEE International Reliability Physics Symposium (IRPS), 2022, pp. P23-1-P23-6, doi: 10.1109/IRPS48227.2022.9764552.
13. L. C. Acharya, A. k. Sharma, V. Ramakrishan, A. Mandal, S. Dasgupta and A. Bulusu, "Variation Aware Timing Model of CMOS Inverter for an Efficient ECSM Characterization," 2021 22nd International Symposium on Quality Electronic Design (ISQED), 2021, pp. 251-256, doi: 10.1109/ISQED51717.2021.9424341.
14. Lalit M. Dani, Neeraj Mishra and Anand Bulusu, “MOS Varactor RO architectures in Near Threshold Regime using Forward Body Biasing techniques,” VLSI Design Conference, January 2019, Delhi.
15. Lalit M. Dani, N. Mishra, S.K. Banchhor, S. Miryala, A. Doneria, Bulusu Anand, “Design andCharacterization of Bulk Driven MOS Varactor Based VCO at Near Threshold Regime,” IEEE-S3S, San Francisco, October 2018.
16. Raghav Chawla, S. Yadav, A. Sharma, B. Kaur, R. Pratap and Bulusu Anand, “TSV Induced Stress Model and Its Application in Delay Estimation,” IEEE-S3S, San Francisco, October 2018.
17. Arvind Sharma, Naushad Alam, Raghav Chawla,Bulusu Anand, “Modeling the effect of variability on the timing response of CMOS inverter-transmission gate structure,” International Symposium on Devices, Circuits and Systems (ISDCS), Howrah.
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20. Archana Pandey, Pitul Garg, Shobhit Tyagi, Rajeev Ranjan, Anand Bulusu, “A Modified Method of Logical Effort for FinFET Circuits considering of Fin-Extension Efforts,” IEEE ISQED-2018.
21. Abhishek Acharya, Sudeb Dasgupta and Bulusu Anand, Impact of Device Design Parameters on VDSAT and Analog Performance of TFETs,” Accepted for presentation in IEEE Silicon Nanoelectronics Workshop 2017.
22. Archana Pandey, Harsh Kumar, Praanshu Goyal, S. K. Manhas, Sudeb Dasgupta, Bulusu Anand “FinFET Device Circuit Co-design Issues: Impact of Circuit Parameters on Delay” , IEEE VLSI Design, 2016.
23. Sayyaparaju Sagar Varma, A. Sharma, Bulusu Anand, "An efficient methodology to characterize the TSPC flip flop setup time for static timing analysis," IEEE SMACD, 2016, Lisbon.
24. Chaudhry Indra Kumar, A. Sharma, S. Miryala, Bulusu Anand, "A novel energy-efficient self-correcting methodology employing INWE," IEEE SMACD, 2016, Lisbon.
25. Arvind Sharma, Neeraj Mishra, Naushad Alam, Sudeb Dasgupta, and Bulusu Anand, "Pre-layout Estimation of Performance and Design of Basic Analog Circuits in Stress Enabled Technologies" in IEEE VDAT, 2015.
26. Yogesh Chaurasiya, Surabhi Bhargava, Arvind Sharma, Baljit Kaur, and Bulusu Anand, "Timing Model for Two Stage Buffer and Its Application in ECSM Characterization", in IEEE VDAT, 2015.
27. Arvind Kumar Sharma, Yogendra Sharma, Sudeb Dasgupta and Bulusu Anand, “Efficient Static D-Latch Standard Cell Characterization Using a Novel Setup Time Model,” Accepted in IEEE ISQED 2015.
28. Parmanand Singh,V. Asthana, R. Sithanandam, A. Bulusu, S. Dasgupta, “Analytical Modeling of Sub-onset Current of Tunnel Field Effect Transistor,” IEEE VLSI Design, 2014.
29. Bijay Kumar Dalai, A. Bulusu, N. Kannan and Arvind Kumar Sharma, "An Empirical Delta Delay Model for Highly Scaled CMOS Inverter Considering Well Proximity Effect," VDAT 2014.
30. Saurabh K. Nema, M. SaiKiran, P. Singh, Archana Pandey, S. K. Manhas, A. K. Saxena, Anand Bulusu, “Improved Underlap FinFET with Asymmetric Spacer Permittivities,” Accepted in IWPSD 2013.
31. Arvind Kumar Sharma, Naushad Alam, Sudeb Dasgupta and Bulusu Anand, “The Impact of Process-Induced Mechanical Stress on D-Latch Timing Performance,” Accepted in IEEE IMPACT 2013.
32. S. Maheshwaram, S.K. Manhas, G. Kaushal, and B. Anand, “Vertical Nanowire MOSFET Parasitic Resistance Modeling,” in Proc. IEEE EDSSC 2013, Hong Kong.
33. Prahlad Kumar Sahu, R. Sithanandam , Anand Bulusu and Sudeb Dasgupta “TCAD Evaluation of Fin Architecture on SOI Substrate and its Comparison with Planar FDSOI MOSFET at 28nm Technology Node”,” VDAT, 2013.
34. Menka, Bulusu Anand and Dasgupta S., “A TCAD approach to evaluate channel electrondensity of double gate symmetric n-tunnel FET”, INDICON 2012, pp:577-581.
35. Baljit Kaur, S. Miryala, S. K. Manhas and Bulusu Anand, “An Efficient Method for ECSM Characterization of CMOS Inverter in Nanometer Range Technologies,” Accepted in IEEE International Symposium on Quality Electronic Design (ISQED) 2013.
36. Archana Pandey, Swati Raycha, Satish Maheshwaram, S. K. Manhas, S. Dasgupta, Bulusu Anand, “Underlap FinFET Capacitance: Impact of Input Transition Time and Output Load” IEEE International Nanoelectronics Conference (INEC) 2013.
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40. Arnab Kumar Biswas, Anand Bulusu and Sudeb Dasgupta*, “*A Proposed Output Buffer at 90 nm Technology with Minimum Signal Switching Noise at 83.3MHz,” Proceedings of IEEE ISVLSI 2011.
41. Sandeep Miryala, Baljeeth Kaur, Bulusu Anand and Sanjeev Manhas, "Efficient Nanoscale VLSI Standard Cell Library Characterization Using a Novel Delay Model," Proceedings of IEEE ISQED 2011.
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44. Pradeep Kumar Chawda, B. Anand, and V.Ramgopal Rao, "Effectiveness of Optimum Body Bias for Leakage Reduction in High K CMOS Circuits", Proceedings of 35th International Conference on Solid State Devices and Materials (SSDM 2004), pp. 434-435, Tokyo, Japan, September 15-17, 2004.
45. Sushant Suryagandh, B. Anand, M. P. Desai and V. Ramgopal Rao, “Dynamic Threshold Voltage CMOS (DTMOS) for Future Low Power Sub-1V Applications," Proceedings of 10th International Workshop on Physics of Semiconductor Devices (IWPSD), pp. 655-658, December 1999, New Delhi.

# Sponsored Projects:

* 1. “Nanoscale FinFET device and circuit design methodology”

PI: Anand Bulusu Sponsor: DST Cost: Rs. 20.40 Lakh Status: Completed

Description: Our aim is to build a quantitative link between device and circuit level performance of FinFETs. We propose to do this by developing models of FinFET device parasitics and using these to develop circuit delay and power models.

* 1. “A robust methodology for nanoscale VLSI circuit design considering layout dependent systematic variations”

PI: Anand Bulusu, Co-PI: Sudeb Dasgupta Sponsor: DST Cost: Rs. 38.37 Lakh Status: Ongoing Description: Our aim in this project is to model timing performance parameters of circuits with layout parameters in CMOS technologies having process induced mechanical stress. Using such models, we would propose methods to improve the performance of circuits in such CMOS technologies.

* 1. “Remote Detection of Humans Trapped Under Debris in Disaster Affected Areas Using RF Sensing of Cardiopulmonary Motion.” (SMPD-C2SD)

PI: Sudeb Dasgupta, Co-PI: Anand Bulusu Sponsor: MIETY (formerly DIETY) Cost: Rs. 5 Cr. Status: Completed

Description: In this project, we propose an RF sensing based system which can identify the number and depths of living persons trapped inside debris due to disasters such as earthquakes etc. The presence of human life can be ascertained by the virtue of its vital signs such as respiration rate and heartbeats. We propose to use a system applying single band RF sensors with on-chip processing. All the parts of the system (except PA and antenna) would be implemented within a CMOS SoC.

* 1. ICT Academy

PI: Sanjeev Manhas Co-PI: Anand Bulusu Sponsor: MIETY (formerly DIETY) Cost: Rs. 7Cr. Status: Ongoing

Description: In this project, the faculty and graduates of academic institutions in Uttarakhand, Himachal and Jammu and Kashmir would be imparted course and skill training.

* 1. Advanced MOS Physics and its application to device modeling (Consultancy)

PI: Anand Bulusu Sponsor: SCL, Chandigarh, ISRO Cost: Rs. 1.7 Lakh Status: Completed

Description: Classes and discussion on advanced MOS physics and modeling for SCL’s CMOS technology.

* 1. Development and Efficient Characterization of Floating Body (FB) and Dynamic Threshold (DT) CMOS Partially Depleted Silicon-On-Insulator (PDSOI) Standard Cell Libraries

PI: Anand Bulusu Sponsor: DST Cost: Rs. 49 Lakhs (Ongoing)

Description: PDSOI technology is being developed in India by SCL Chandigarh for its radiation hard nature. The project aims for the design enablement of the PDSOI technology and its early circuit design for process and PDK improvement. We will consider the PDSOI floating body effects rigorously.

* 1. An energy efficient IoT processor build using an optimized near-threshold voltage s tandard cell library

PI: Anand Bulusu Sponsor: IMPRINT-2 (DST) Cost: Rs. 54 Lakhs (Ongoing)

Description: This project involves the development of a near threshold standard cell library an IoT processor in a 28 nm CMOS process and in SCL’s 180 nm CMOS process.

* 1. A robust and scalable VLSI characterization methodology for high performance CMOS designs considering spatial and temporal variations

PI: Anand Bulusu Sponsor: Semiconductor Research Corporation (SRC) Cost: $48000 (Ongoing)

Description: Timing models of planar CMOS standard cells would be developed. These would estimate spatial and temporal variations through Vth, μ0 and RCs. These are then used to develop an aging-aware and PVT variability aware STA flow.

* 1. A Design Methodology of Compute-In-Memory SRAM Macro for AI/ML Applications

PI: S. Dasgupta Co-PI: Anand Bulusu Sponsor: Semiconductor Research Corporation (SRC) Cost: $36000 (Ongoing)

Description: Circuit design methodology for analog compute-in-memory circuits considering PVT variations.

* 1. Development of 1.8/5V/10V/20V I/O Pads in SCL’s 0.18µm CMOS Process

 PI: S. Dasgupta Co-PI: Anand Bulusu Sponsor: ISRO Cost: Rs. 38 Lakhs (Ongoing)

* 1. Design and Development of ROM based low power Al Inference chip

PI: Anand Bulusu Sponsor: TIH Cost: 90 Lakhs (Ongoing)

* 1. A PDSOI Analog Cell Library Consisting 2 Stage OPAMPS And Comparators Designed Considering Floating Body And Self Heating Effects

PI: Anand Bulusu Sponsor: ISRO Cost: Rs. 14 Lakhs

* 1. Smart Contactless Technology Development For Smart Fencing (Multi-Institutional)

PI: Anand Bulusu (IITR) Sponsor: DST Cost: Rs. 22 Lakhs (IITR)

# Visits/Awards:

# Visited Forschungszentrum, Julich, Germany in June – July (2 months) 2018 under DAAD Bilateral Faculty Exchange Program to collaborate on Negative Capacitance FETs and TFETs. My German collaborator, Prof. Q-T. Zhao, visited IIT Roorkee in December 2018.

# Bilateral Faculty Exchange Program under ASEM-DUO program with Prof. Arian Ionescu, EPFL, Lousanne, Switzerland, July-August 2022.

# Talk in KU, Leuven, July, 2022: “Aging aware STA methodology for path level timing performance of digital circuits”.

# Talk in EE, Purdue University, March 2022: “Circuit design methodologies for emerging devices”.

# Talk in EE, University of California, Berkeley, March 2022: “NCFET: Towards a Systematic Circuit Design”.

# Talk in Texas Instruments, Bangalore, November 2022, “Aging aware STA methodology for path level timing performance of digital circuits”.

# Invited talk in VLSI Design Conference 2023, Hyderabad, “Variability aware timing analysis considering device/layout level phenomena at circuit level abstraction”.

# Talk at EPFL, Lausanne, Switzerland, “Towards Reliable Circuits Using NC/FeFETs”.

# Ph.Ds Supervised:

|  |  |  |
| --- | --- | --- |
| **Area** | **Scholar Name** | **Status of Ph.D** |
| FeFET CIM Design | Abhishek Goel | Ongoing |
| PDSOI RF Switch device-circuit co-design | Narendra Pratap Singh | Ongoing |
| Mixed Signal Design | Ravi | Ongoing |
| FeFET Memory design | Abhishek Kumar |  Ongoing |
| Energy Harvesting System and Power Management Circuits | Kartikay Mani Tripathi | Ongoing |
| Circuits for compute-in-memory | Neha Gupta | Ongoing |
| Variation Aware Efficient Standard Cell Characterization | Lomash Chandra Acharya | Ongoing |
| NCFET Device Circuit Interaction |  Amit Kumar Behera | Ongoing |
| Near Threshold Standard Cell Design |  Mahipal Dargupally | Ongoing |
| NC-Tunnel FET Device Circuit Interaction | Khoirom Johnson | Ongoing |
| Radiation Hard Circuit Design at Cryogenic Temperature | Ashutosh Yadav | Ongoing |
| Analog Circuit Design in PDSOI Technologies | H S Jattana | Ongoing |
| Circuit Design for In-Memory Computation | Dinesh Kushwaha | Ongoing |
| NCFET Device-Circuit Interaction | Nitanshu Chauhan | Awarded | NITU |
| Tunnel FET Device-Circuit Interaction | Abhishek Acharya | Awarded | NIT Surat |
| FinFET Device-Circuit interaction (Analog Domain) | Shashank Bancchor | Awarded | Intel |
| FinFET Device-Circuit interaction in Near Threshold Digital Domain | Sarita Yadav | Awarded | NITU |
| CMOS PLL Design | Neeraj Mishra | Awarded | IMEC Belgium |
| Low Voltage CMOS VCO Design | Lalit Dani | Awarded | Global Foundries, Bangalore |
| Near Threshold CMOS Digital Circuit Design and Analysis | Inder Chaudhary | Awarded | DTU |
| Mechanical Stress Aware Nanoscale VLSI Circuit Design Methodologies | Arvind Sharma | Awarded | IMEC, Belgium |
| Archana Pandey | Awarded | Jaypee |
| Modeling of FinFET device parasitics |
| Menaka | Awarded | NIT Jaipur |
| TunnelFET device-circuit co-design |
| Satish Maheshwaram | Awarded | NIT Warangal |
| Device-circuit co-design of Silicon Nanowire transistor |
| Baljit Kaur | Awarded | NIT Delhi |
| Performance models for nanoscale VLSI circuits |
| Naushad Alam | Awarded | AMU |
| Robust circuit design methodology for nanoscale VLSI technologies |
|  |  |

 **Ph.D Thesis:**

## Evaluating DTMOS in solving the voltage scaling problem: A circuit performance perspective

**Supervisor:** Prof. Madhav P. Desai, EE Department, IIT Bombay.

Increasing circuit speed by scaling is resulting in the problem of exponentially increasing the leakage power in sub-1V technologies. One of the proposed solutions to this problem is Dynamic-Threshold-MOSFET (DTMOS), which is also compatible with conventional CMOS technology. In DTMOS, a forward bias is applied to the body of a MOSFET when it is ON. This results in an increased drive current in a DTMOS device while the leakage current is not affected. However, a study of its impact at the circuit level, while considering the DTMOS device bodies in detail, has not been done thus far. In this work we compare the performance of an optimized DTMOS circuit with that of its conventional equivalent while considering the loading and parasitic effects of the DTMOS device body. We first optimize the DTMOS device design such that circuit performance is maximized. For this, we propose a novel figure-of-merit (FoM) for the device and show that by optimizing this FoM we obtain device design parameters which maximize logic gate performance. We must now compare the projected performance of DTMOS and conventional implementations of an arbitrary logic circuit. For this, we derive simple but accurate delay and input capacitance models for DTMOS logic gates. These delay models incorporate the effect of the body parasitics, and can be used to project the behaviour of logic circuits. Thus, in our work, we establish a quantitative link between DTMOS device performance and circuit level performance. Based on this approach, in a 50nm drawn gate length technology, we conclude that DTMOS is a *partial* solution to the voltage scaling problem and can be used to reduce the leakage power significantly if an overhead in area can be tolerated. We also observe that in PDSOI technology, the DTMOS device can be more effective than the body-tied-to-source device in eliminating the floating body (FB) and kink effects, if the area overhead can be tolerated.

# Pre-IITR Research Experience:

* Jul 2006 – March 2007 (Indian Institute of Technology, Bombay)

**Project Name** Comparison of performance of CMOS and NMOS technologies

**Designation** Senior Research Engineer

**Supervisor** Prof. V. Ramgopal Rao

**Description** With technology scaling the static power consumption of CMOS has already become about half of the total power consumption. The simpler NMOS technology, which was discarded due to its static current, thus becomes relevant again. The aim of this project is to explore if NMOS logic can reduce power consumption as compared to CMOS. This involves optimizing threshold voltages of devices for NMOS logic, optimizing NMOS circuits and comparing representative NMOS and CMOS circuits.

* + - March 2007 – April 2008 (Freescale Semiconductor India Pvt. Ltd.)
		- **Project Name** A metric for sensitivity of standard cells to process variations

**Designation** Senior Design Engineer

**Supervisor** Dr. Surya Veeraraghavan and Dr. Bhuwan Agarwal

**Description** The standard cell library is characterized (for all process corners) early on in the design cycle in today’s modern technologies. However, even at a technology node, process parameters keep changing due to a gradual “maturing” of technology. It is not possible to repeatedly perform the characterization of standard cell libraries as the process matures. The aim of this project is to propose a “metric” for each standard cell, which can give a “measure” of sensitivity of its delay/power characteristics to process variations at each corner.

* + - November 2007 – February 2008 (Freescale Semiconductor India Pvt. Ltd.)

**Project Name** Optimum standard cell design in sub-100nm CMOS LP technologies

**Designation** Senior Design Engineer

**Supervisor** Dr. Surya Veeraraghavan and Dr. Bhuwan Agrawal

**Description** With CMOS technology scaling beyond 100nm, several second-order effects, such as well-proximity, narrow width or stress effects become important. In Low Power (LP) CMOS, technologies, the value of local interconnect capacitance is also larger relative to other contributors. Due to these effects, traditional design and layout methodologies for standard cell library fail to produce desired performance. We proposed a method of standard cell design and layout for sub-100nm LP CMOS technologies.

* + - March 2008 – November 2008 (Freescale Semiconductor India Pvt. Ltd)

**Project Name** Impact of WPE and sress effects in 45nm CMOS circuits

**Designation** Senior Design Engineer

**Supervisor** Dr. Surya Veeraraghavan and Dr. Bhuwan Agrawal

**Description** Starting from 65nm bulk and PDSOI CMOS technologies, MOSFET instance parameter related to Well-Proximity Effect (WPE), stress effect and polysilicon corner rounding are being extracted from layout. However, this increases the time of extraction significantly. In this project, we would study the circuit impact of these effects from measured Silicon data obtained from several ring-oscillators in a test-chip. Our goal is to propose cases, if any, in which the extraction of these parameters is not needed.

# Collaboration/Joint Work with Industry:

|  |  |
| --- | --- |
| **Topic** | **Organisation** |
| Process variation aware Standard Cell extraction | Freescale Semiconductor India Pvt. Ltd. |
| Tunnel FET Device Modeling | ST Microelectronics |
| CMOS VCO Design | ST Microelectronics |
| High Speed Circuits | Global Foundries |
| SRAM Memory Reliability | ARM |
| AI Chip Design | Proficient Design LLC, USATsilicon, Bangalore |
| Near Threshold Voltage Library Design | Einfochips, SCL Chandigarh, Tsilicon |
| Aging Aware STA | Texas Instruments |
| Time to Digital Circuits | Global Foundries |
| PDSOI standard cell library | SCL Chandigarh |
| PDSOI Analog Cells | SCL Chandigarh |

**Teaching Experience:**

* Low Voltage CMOS Circuit Operation (newly designed PG Elective)
* Digital VLSI Circuit Design (PG Elective)
* Analog VLSI Circuit Design (PG Elective)
* Analog Circuits (UG Core)
* Semiconductor Devices (UG Core)
* Fundamentals of Microelectronics (UG Elective)
* Fundamentals of Electronics (UG Core)
* Network Theory (UG Core)
* Automatic Control Systems (UG Core)

# Other Relevant Experience

* Designed a test chip using 65 nm bulk ST Microelctronics PDK for validating our systematic variability aware circuit design techniques.
* Designed a 0.25µm bulk technology *test-chip* with DTMOS circuits. The chip also contained test circuits to validate a technique for interconnect coupling capacitance measurement (CBCCM). The test-chip was fabricated by TSMC and was characterized in IIT Bombay.
* Worked with SPICE, process simulators (TSUPREM4, ISE-DIOS, 3-D TAURUS PROCESS), device simulators (MEDICI, ISE-DESSIS), Layout Editors (MAGIC and Cadence Virtuoso), Schematic Editors, Layout-vs.-Schematic tools.
* Reviewer of research publications for in IEEE Transactions on Electron Devices, IEEE Electron Device Letters, IEEE Transactions on CAS1, IEEE Transactions on TCAD, ISLPED, ISCAS, A-SSCC, VLSI Design Conference etc
* Faculty advisor of IEEE Student Branch, IIT Roorkee and IEEE CAS Student Chapter, IIT Roorkee.

# Pre-Ph.D Work Experience

* October 1995 - June 1996 (Geonics India Pvt. Ltd., Mumbai)

**Designation**: Engineer

**Description**: My job was to maintain and assist in designing marine instrumentation systems for laying underwater pipelines in the Gulf of Kutch.

* February 1998 – October 1998 (IBM Global Services India Pvt. Ltd., Bangalore)

**Designation**: Design Engineer

**Description**: I was responsible for modifying the layout of 0.35μm standard cell library cells after the technology was improved to use Copper interconnect instead of the earlier Aluminum interconnect lines.

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